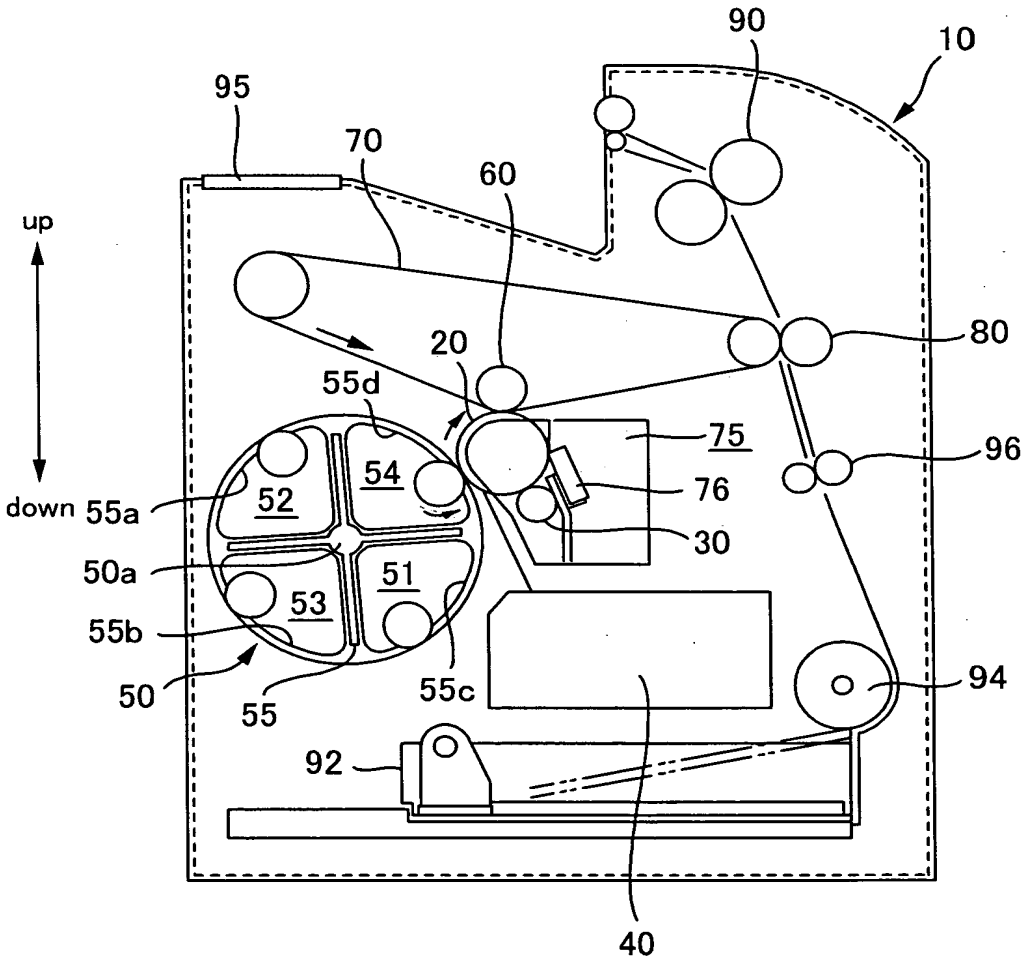

90
10
95
70
60
up
20
80
55d
75
96
54
52
76
down
55a
30
50a
51
53
55b
94
50
55
55c
92
40

FIG. 1

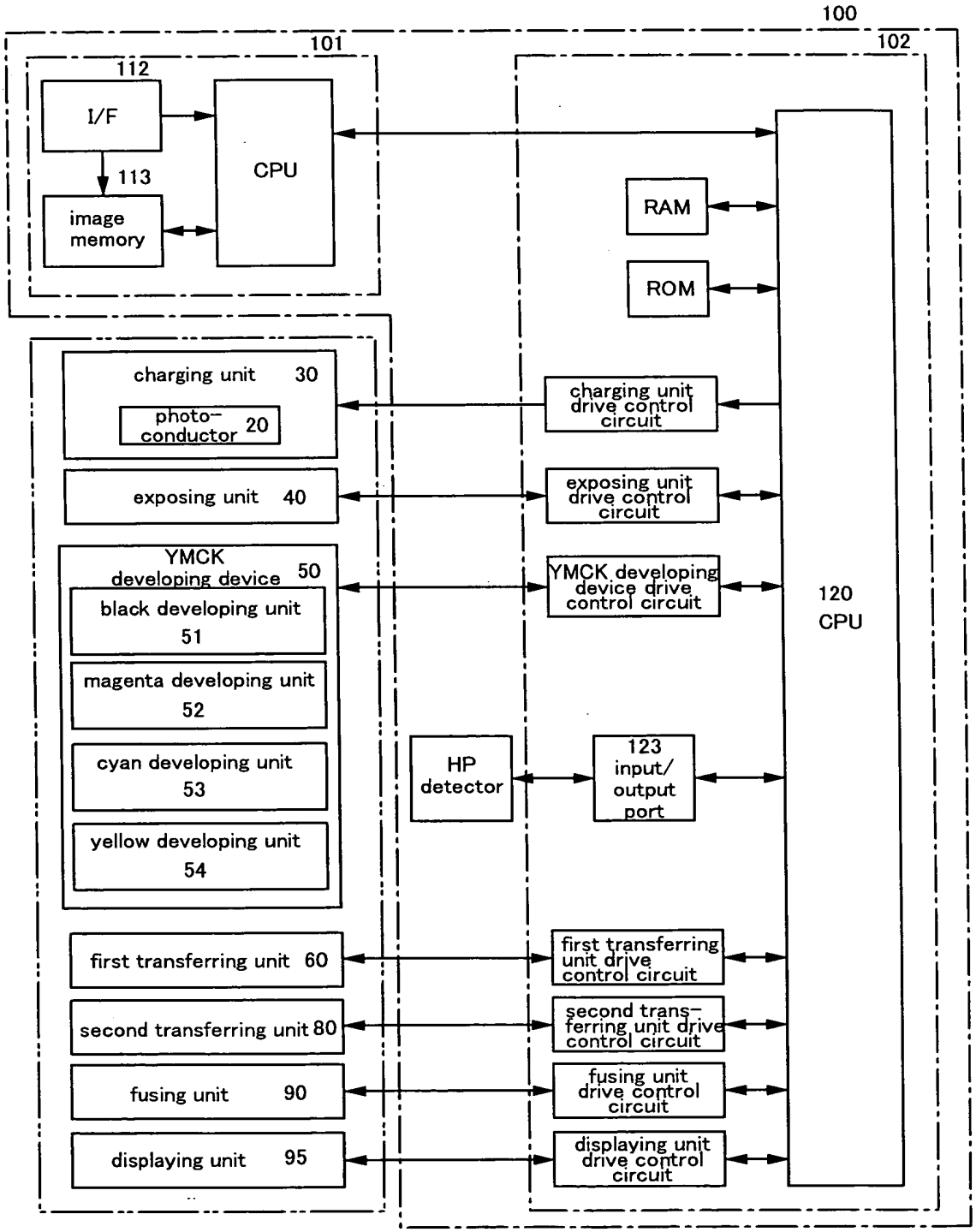

100
101
102
112
I/F
113
image memory
CPU
RAM
ROM
charging unit 30
photo-conductor 20
exposing unit 40
YMCK developing device 50
black developing unit 51
magenta developing unit 52
cyan developing unit 53
yellow developing unit 54
first transferring unit 60
second transferring unit 80
fusing unit 90
displaying unit 95
charging unit drive control circuit
exposing unit drive control circuit
YMCK developing device drive control circuit
HP detector
123 input/output port
first transferring unit drive control circuit
second transferring unit drive control circuit
fusing unit drive control circuit
displaying unit drive control circuit
120 CPU

FIG. 2

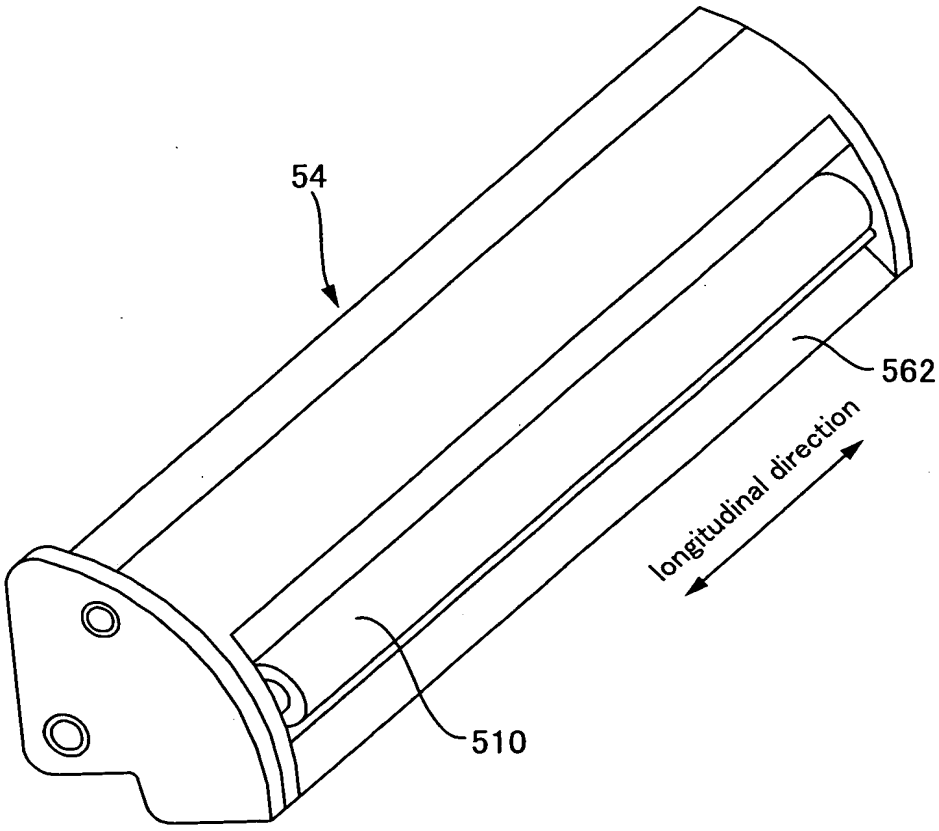


FIG. 3

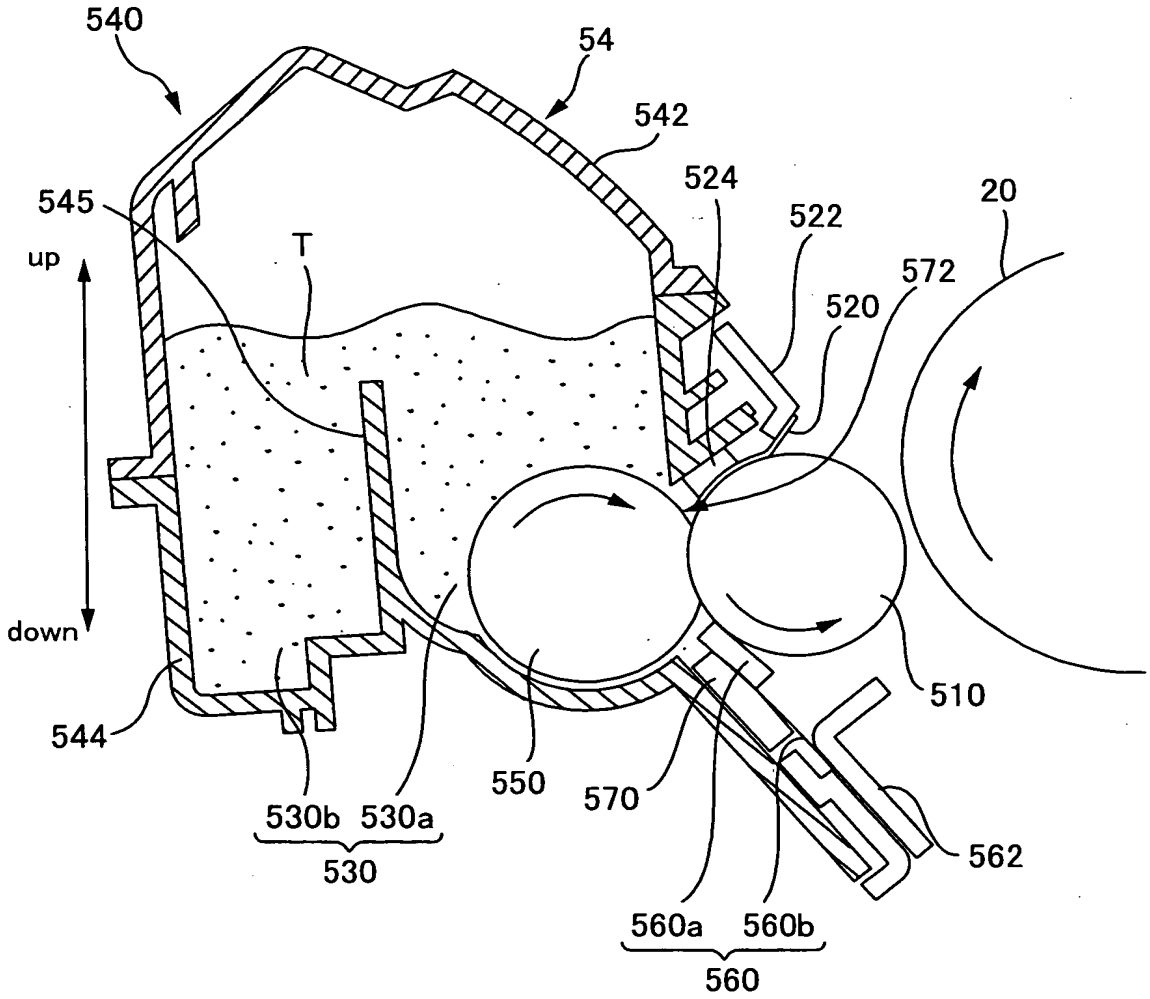

540
54
542
524
522
20
545
T
572
520
up
down
544
510
550
570
530b
530a
530
562
560a
560b
560

FIG. 4

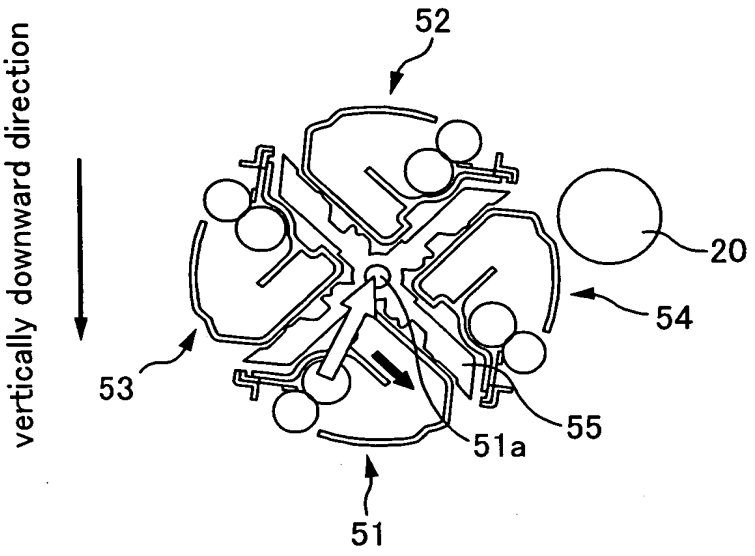

vertically downward direction
52
20
54
53
55
51a
51

FIG. 5A

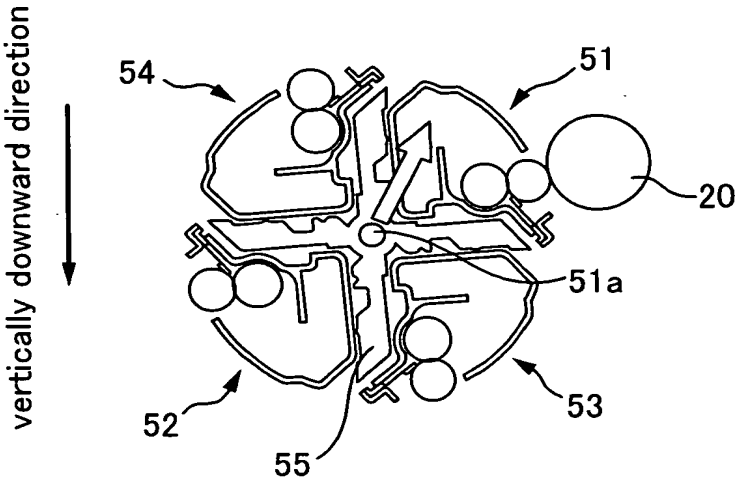

vertically downward direction
54
51
20
51a
52
53
55

FIG. 5B

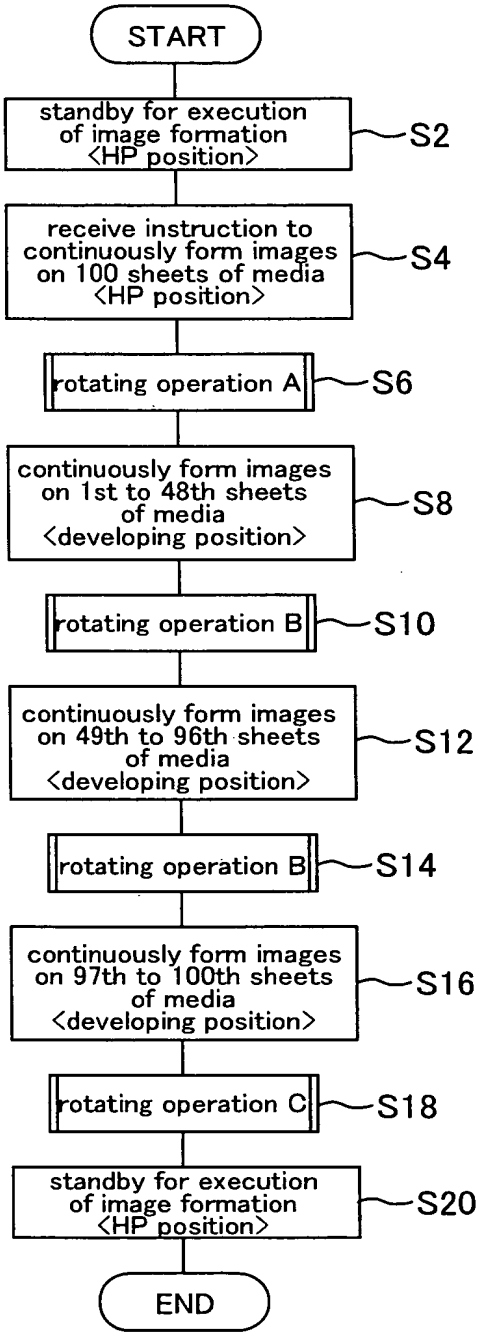

START
standby for execution of image formation <HP position>
S2
receive instruction to continuously form images on 100 sheets of media <HP position>
S4
rotating operation A
S6
continuously form images on 1st to 48th sheets of media <developing position>
S8
rotating operation B
S10
continuously form images on 49th to 96th sheets of media <developing position>
S12
rotating operation B
S14
continuously form images on 97th to 100th sheets of media <developing position>
S16
rotating operation C
S18
standby for execution of image formation <HP position>
S20
END

FIG. 6A

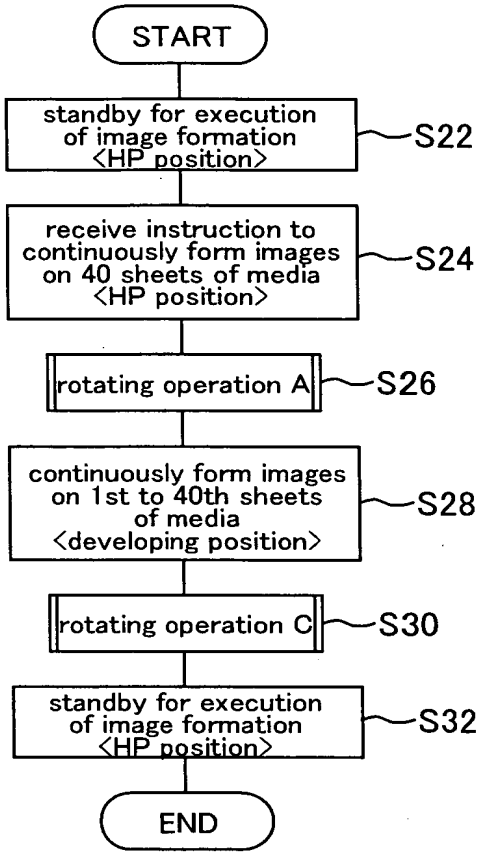

START
standby for execution of image formation <HP position>
S22
receive instruction to continuously form images on 40 sheets of media <HP position>
S24
rotating operation A
S26
continuously form images on 1st to 40th sheets of media <developing position>
S28
rotating operation C
S30
standby for execution of image formation <HP position>
S32
END

FIG. 6B

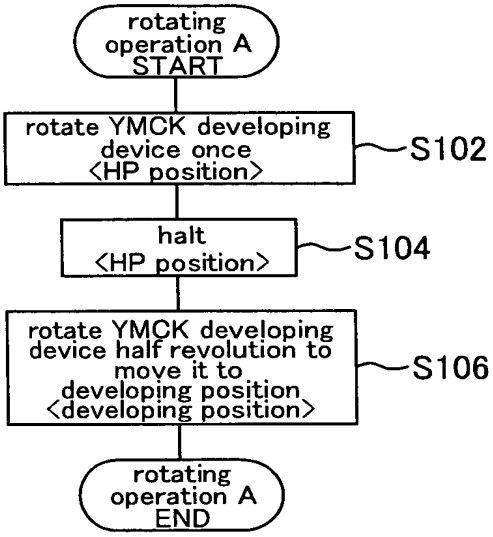


FIG. 7A

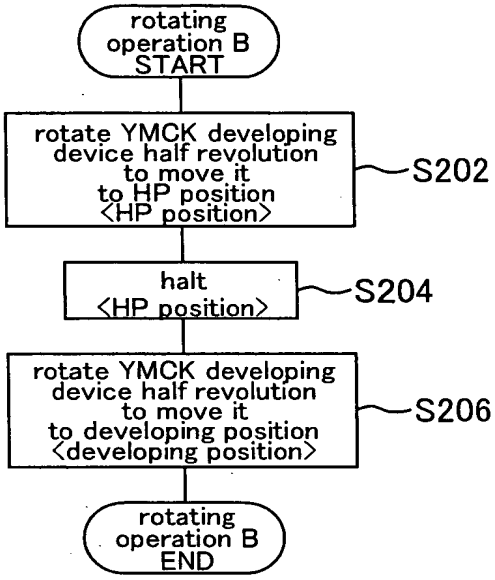


FIG. 7B

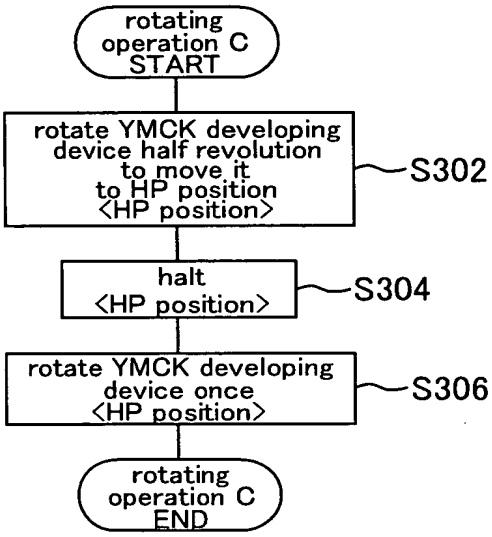


FIG. 7C

	N number of sheets(sheets)	start (times)	middle (times)	end (times)	total M (times)	M/N (times/sheet)
present example	100	1.5	2	1.5	5	0.05
	40	1.5	0	1.5	3	0.075
compara-tive example	100	0.5	2	0.5	3	0.03
	40	0.5	0	0.5	1	0.025

FIG. 8

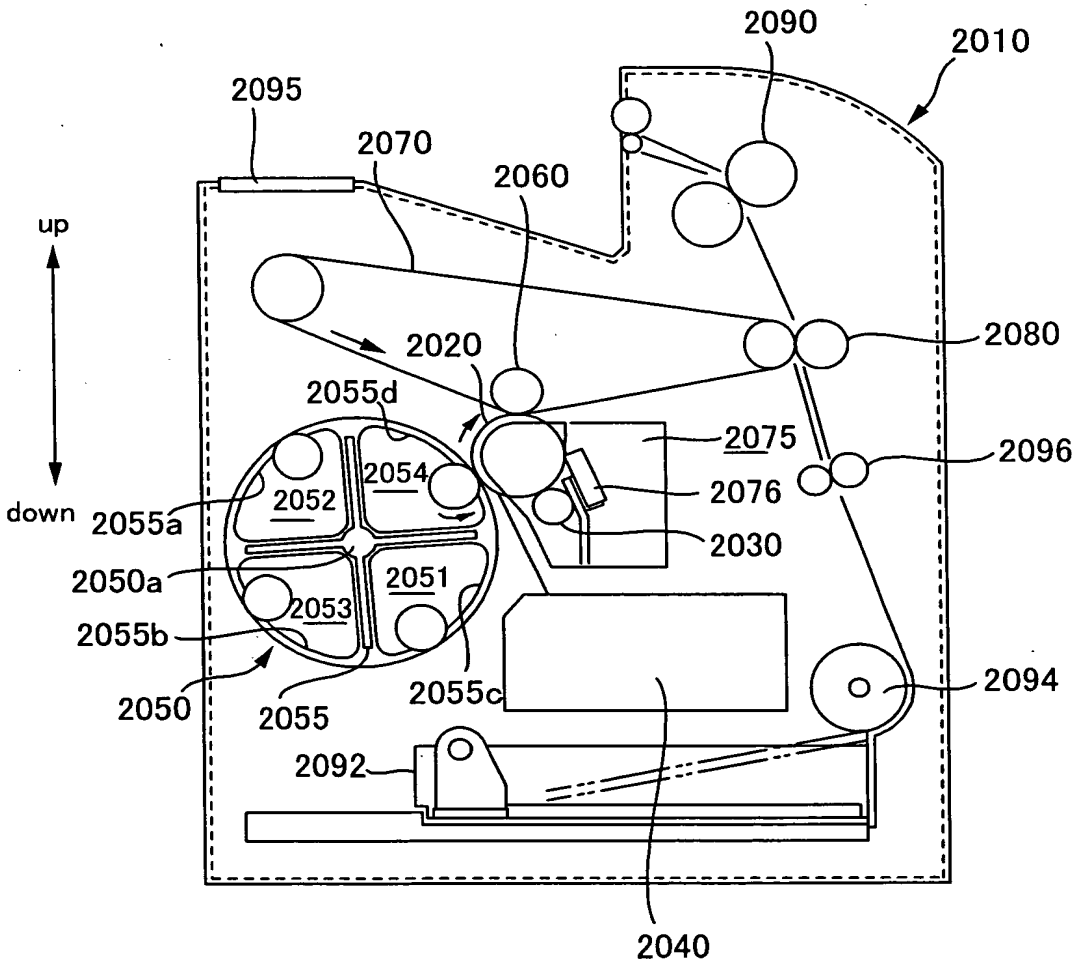

2090
2010
2095
2070
2060
up
down
2080
2020
2055d
2075
2096
2054
2052
2076
2055a
2030
2050a
2051
2053
2055b
2094
2050
2055
2055c
2092
2040

FIG. 9

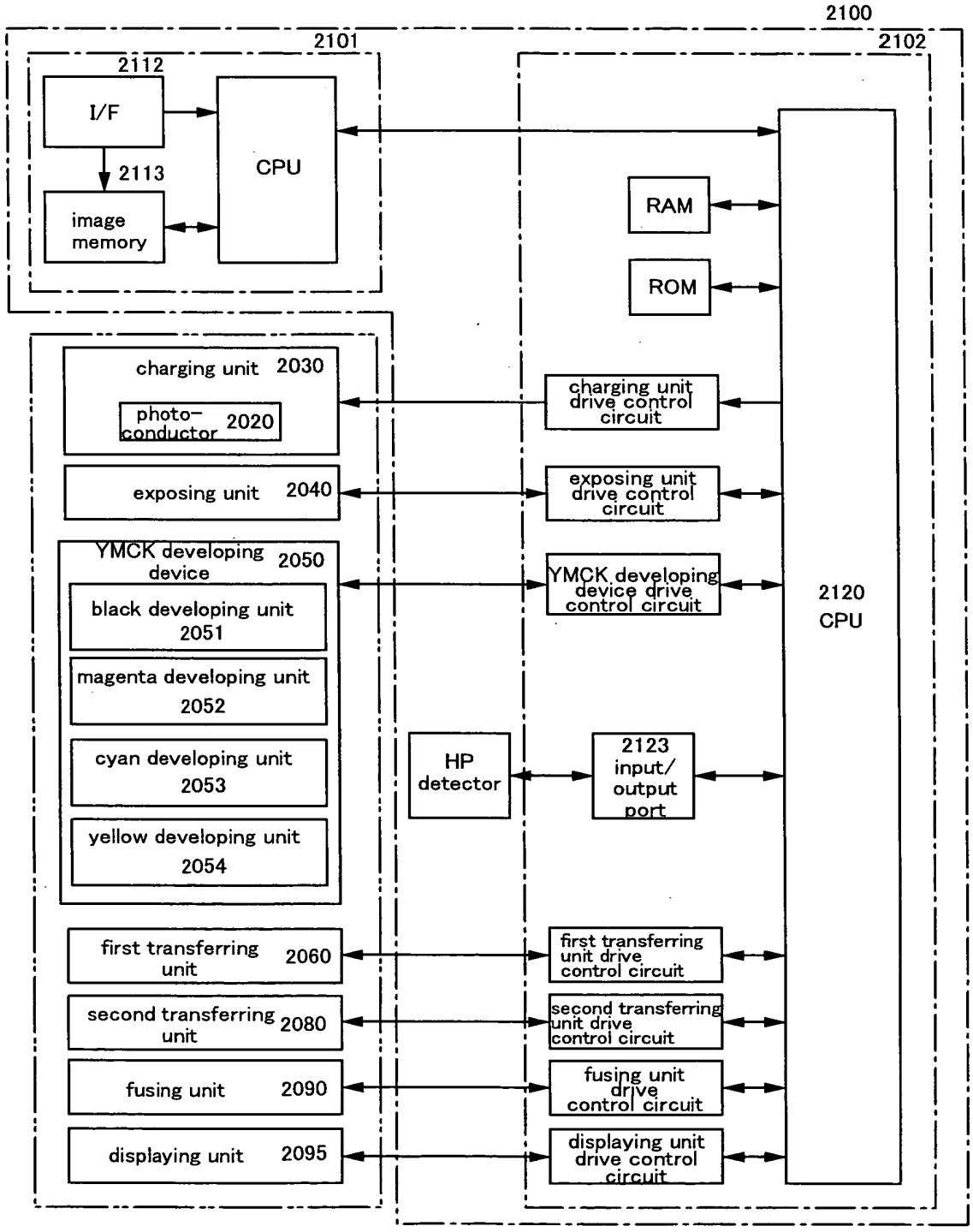

2100
2101
2102
2112
I/F
2113
image memory
CPU
RAM
ROM
charging unit 2030
photo-conductor 2020
charging unit drive control circuit
exposing unit 2040
exposing unit drive control circuit
YMCK developing device 2050
black developing unit 2051
magenta developing unit 2052
cyan developing unit 2053
yellow developing unit 2054
YMCK developing device drive control circuit
2120 CPU
HP detector
2123 input/output port
first transferring unit 2060
first transferring unit drive control circuit
second transferring unit 2080
second transferring unit drive control circuit
fusing unit 2090
fusing unit drive control circuit
displaying unit 2095
displaying unit drive control circuit

FIG. 10

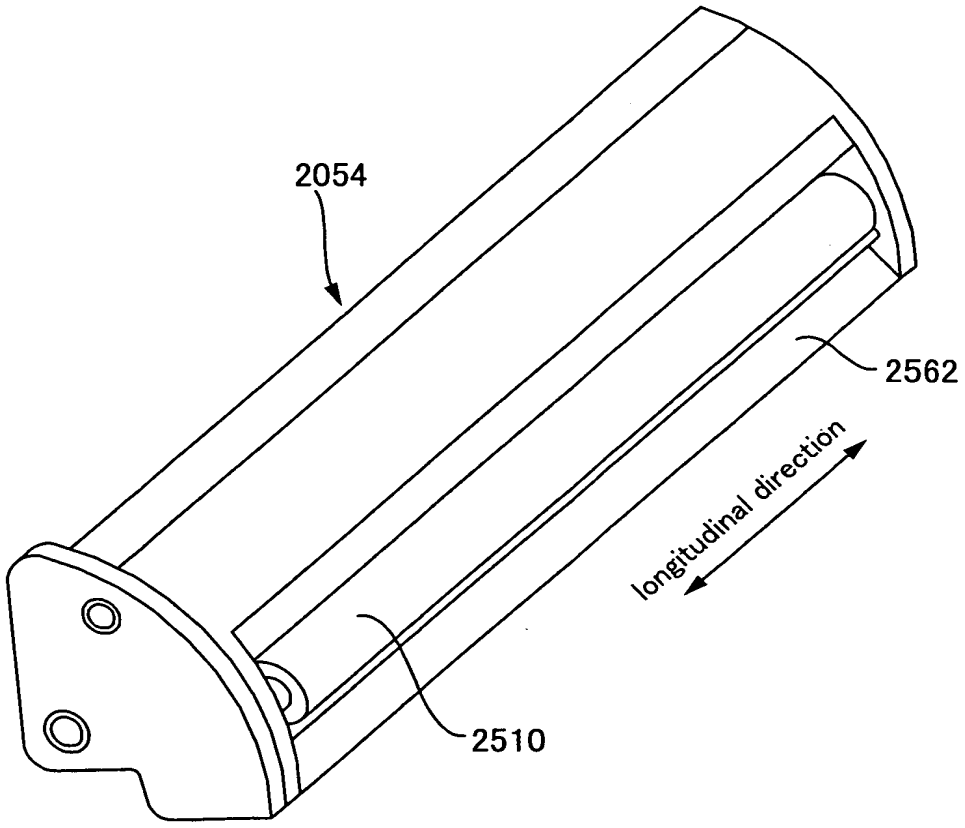


FIG. 11

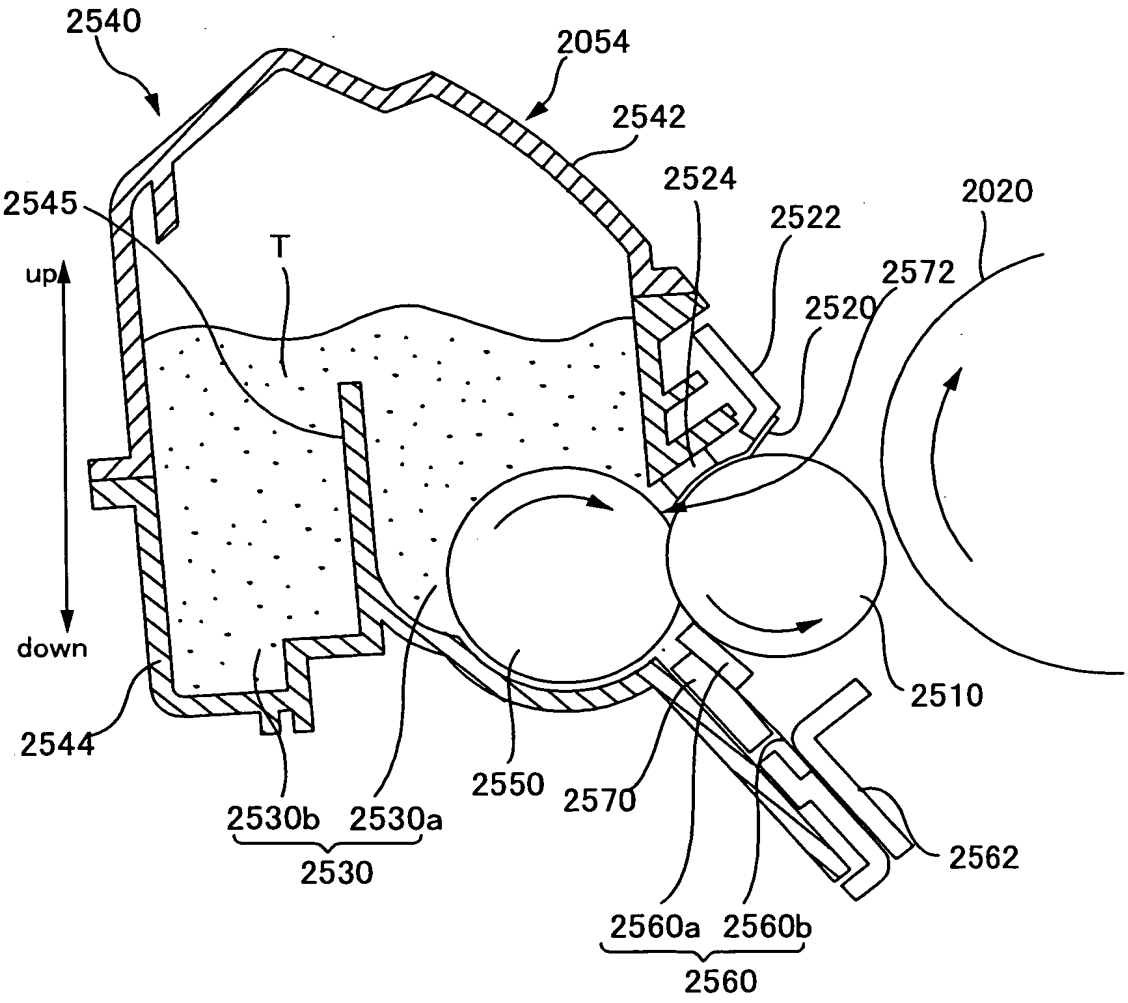

2540
2054
2542
2524
2020
2545
2522
T
2572
up
2520
down
2510
2544
2550
2570
2530b
2530a
2530
2562
2560a
2560b
2560

FIG. 12

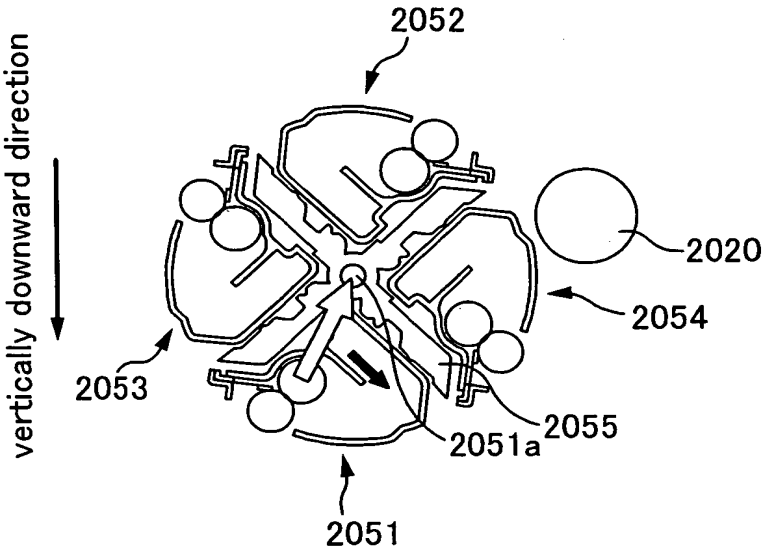


FIG. 13A

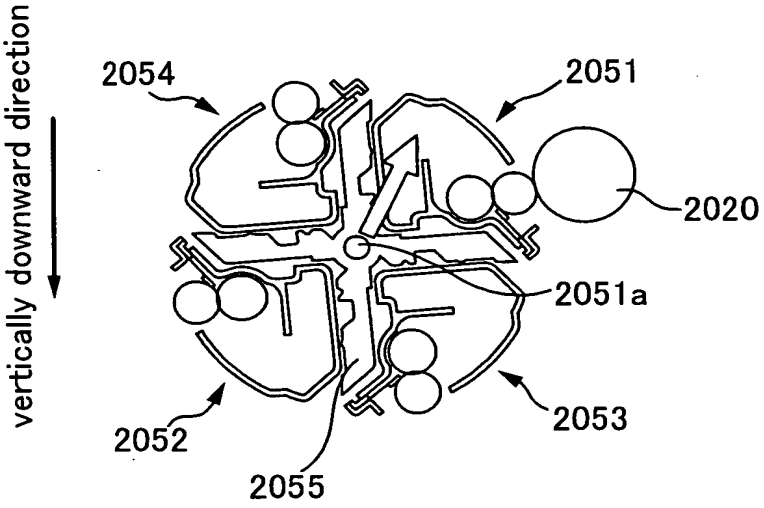


FIG. 13B

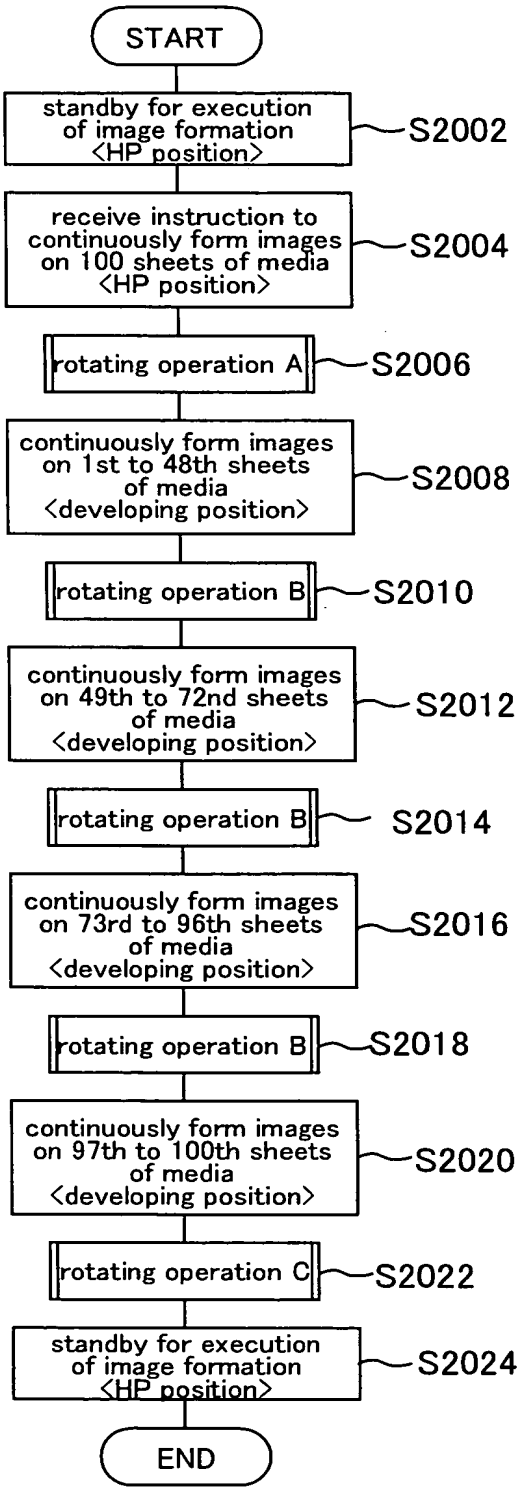


FIG. 14A

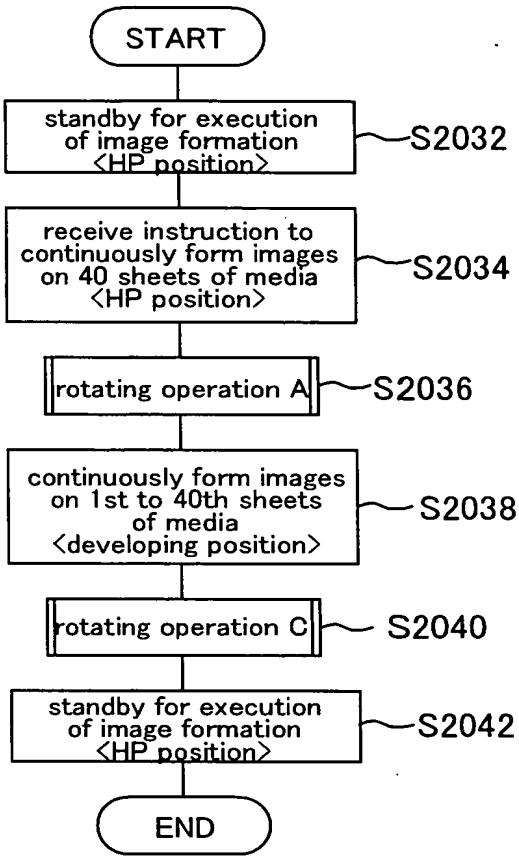


FIG. 14B

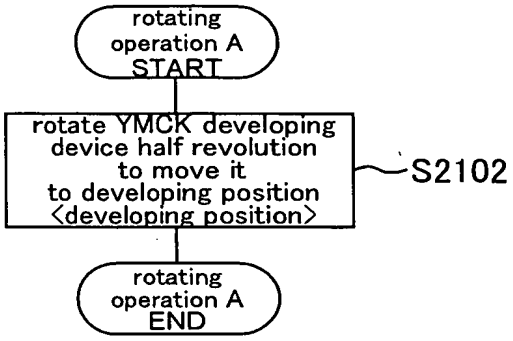


FIG. 15A

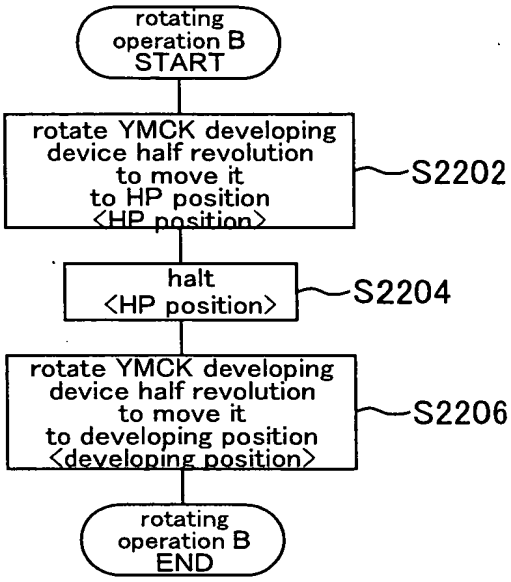


FIG. 15B

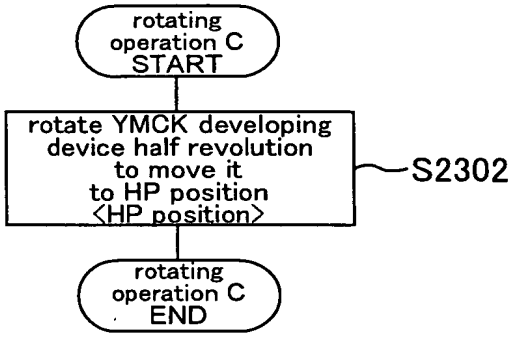


FIG. 15C

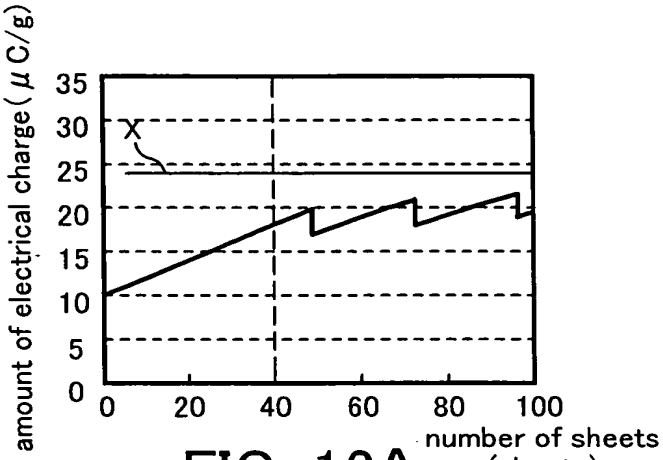


FIG. 16A

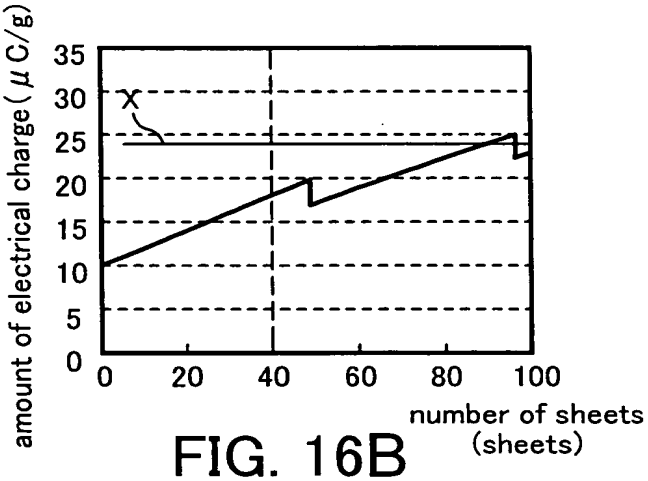


FIG. 16B

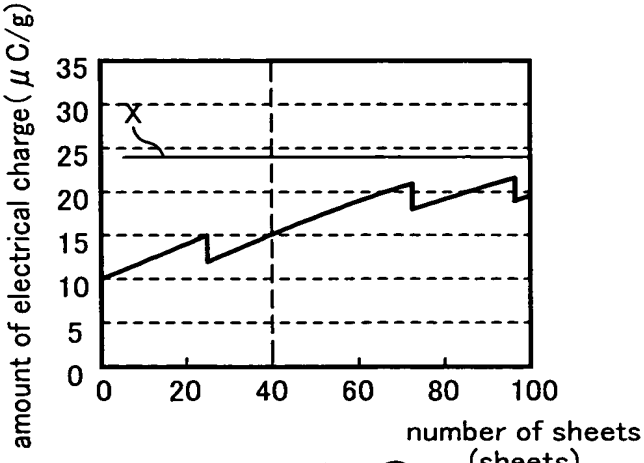


FIG. 16C

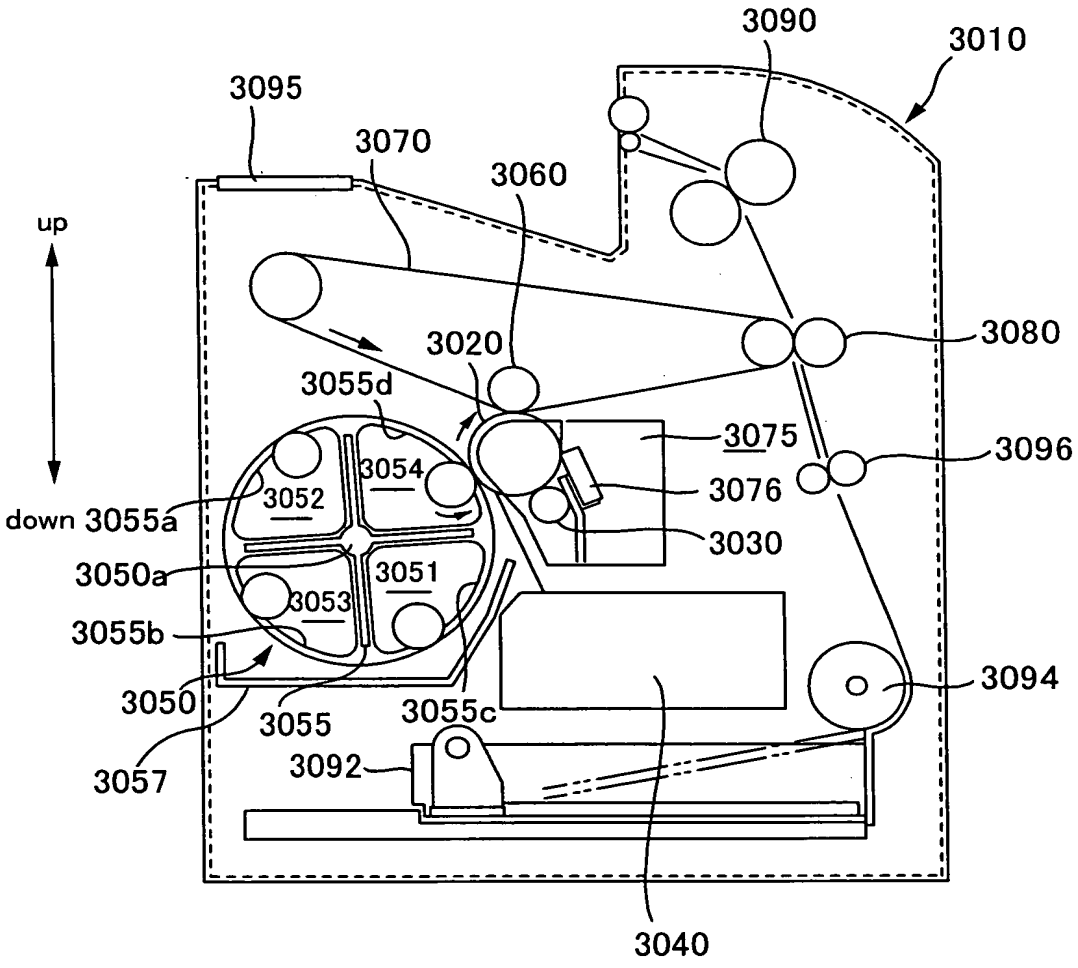

3090
3010
3095
3070
3060
up
3080
3020
3055d
3075
3096
3054
3052
3076
down 3055a
3030
3050a
3051
3053
3055b
3094
3050
3055
3055c
3092
3057
3040

FIG. 17

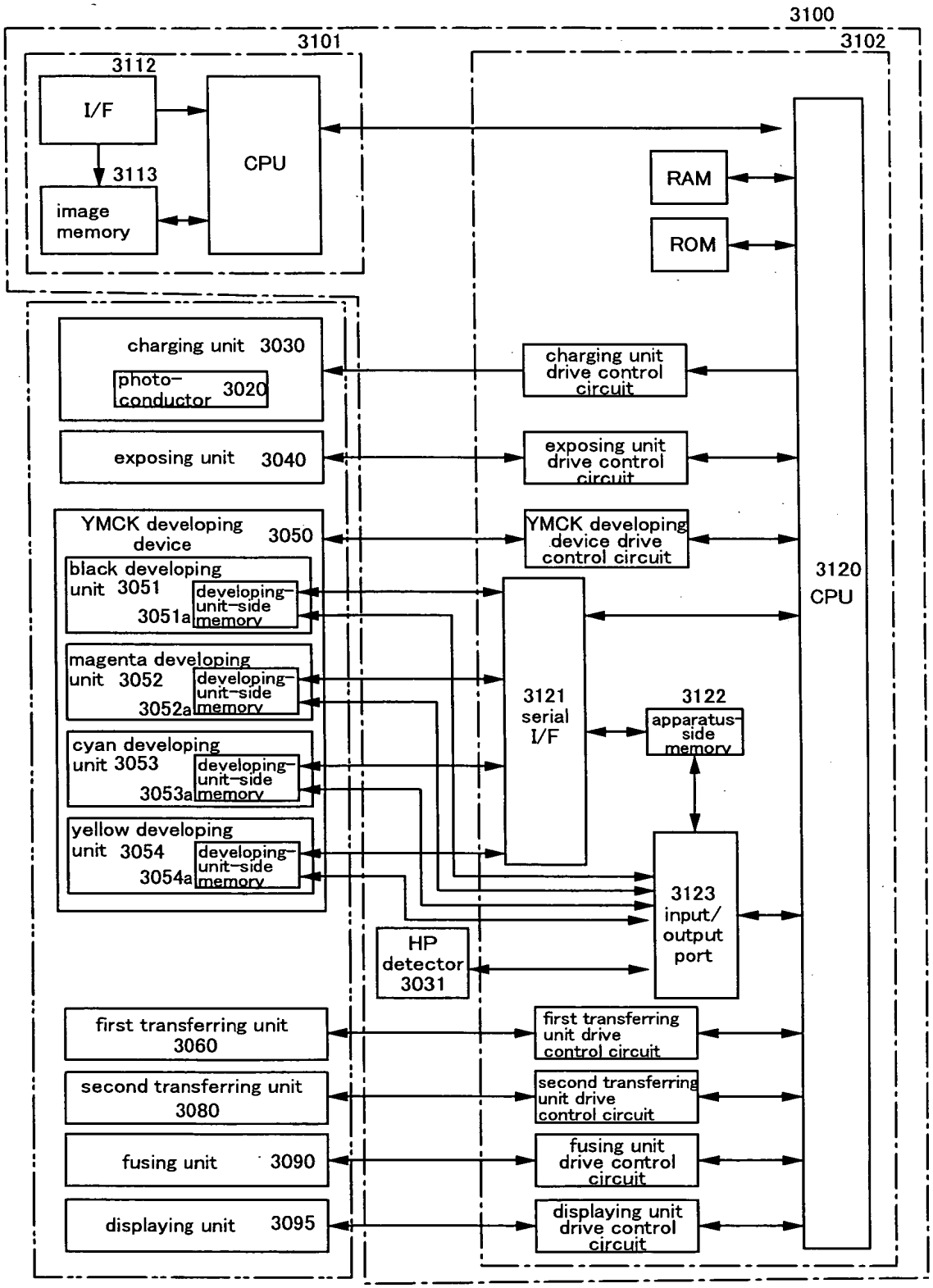

3100
3101
3102
3112
I/F
3113
image memory
CPU
RAM
ROM
charging unit 3030
photo-conductor 3020
exposing unit 3040
YMCK developing device 3050
black developing unit 3051
3051a
developing-unit-side memory
magenta developing unit 3052
3052a
cyan developing unit 3053
3053a
yellow developing unit 3054
3054a
charging unit drive control circuit
exposing unit drive control circuit
YMCK developing device drive control circuit
3120 CPU
3121 serial I/F
3122
apparatus-side memory
3123 input/output port
HP detector 3031
first transferring unit 3060
second transferring unit 3080
fusing unit 3090
displaying unit 3095
first transferring unit drive control circuit
second transferring unit drive control circuit
fusing unit drive control circuit
displaying unit drive control circuit

FIG. 18

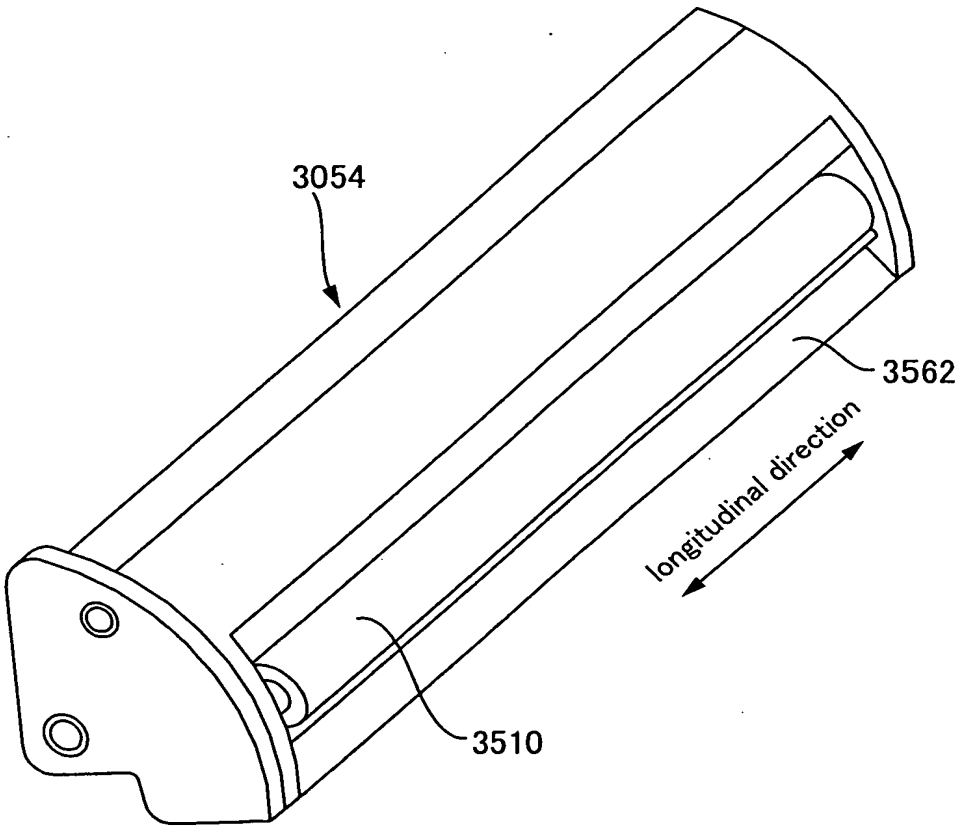


FIG. 19

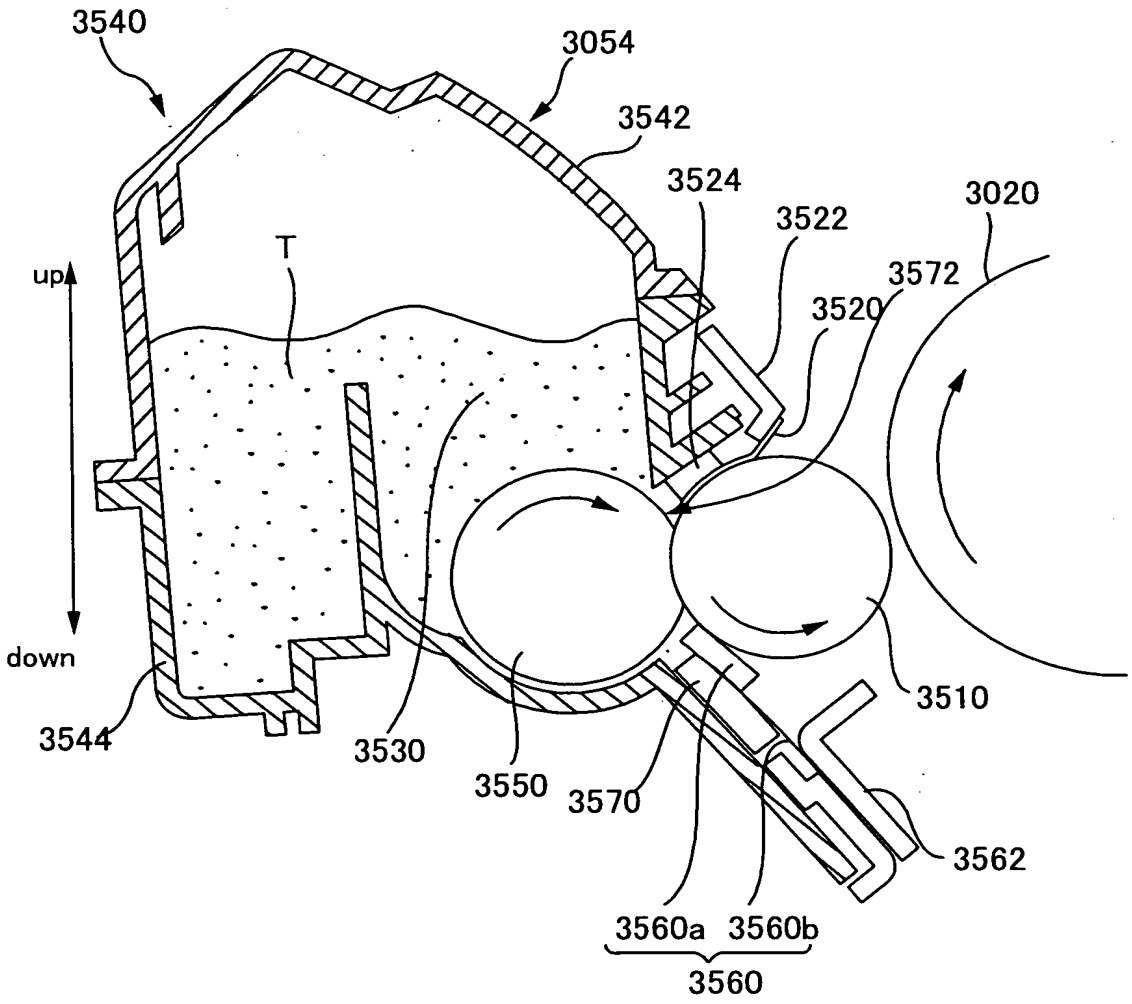

3540
3054
3542
3524
3522
3020
3572
3520
T
up
down
3544
3530
3550
3570
3510
3562
3560a
3560b
3560

FIG. 20

FIG. 21A

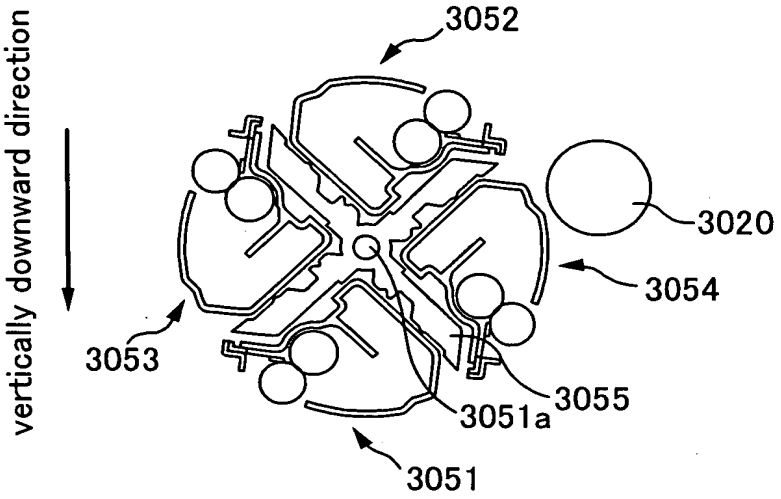


FIG. 21B

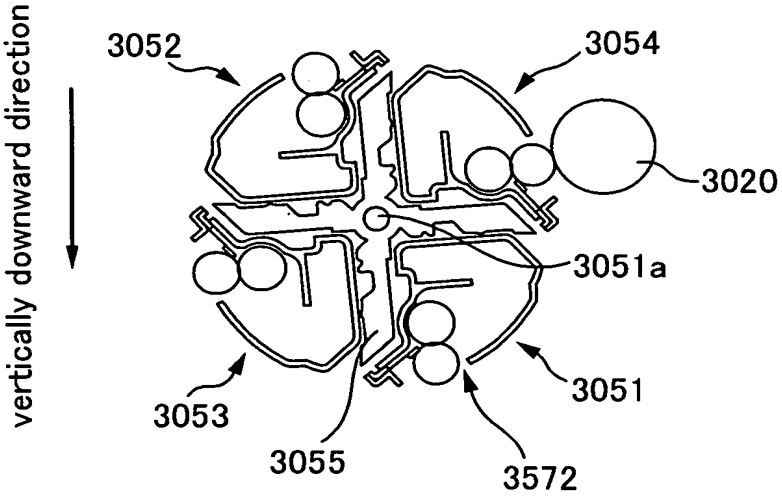


FIG. 21C

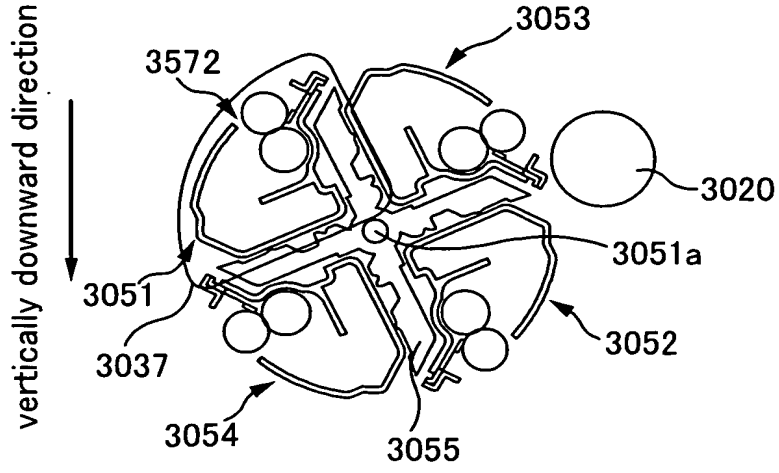


FIG. 22A

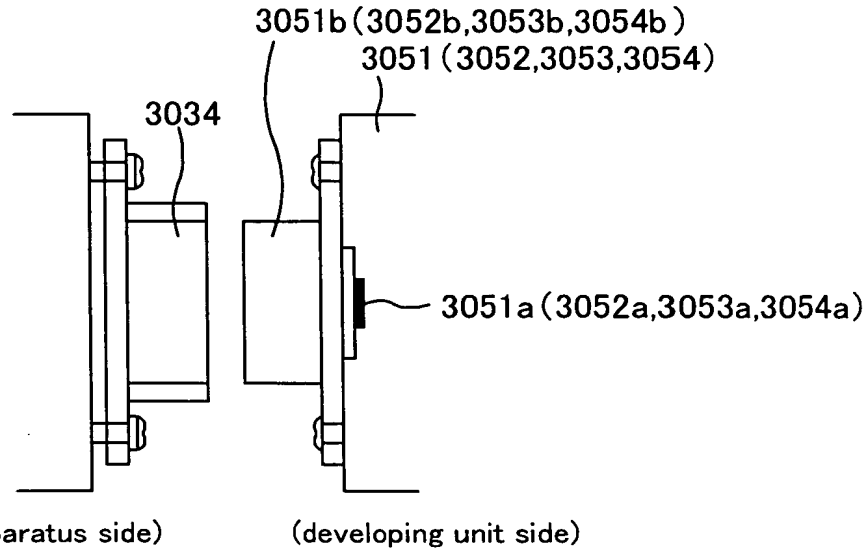
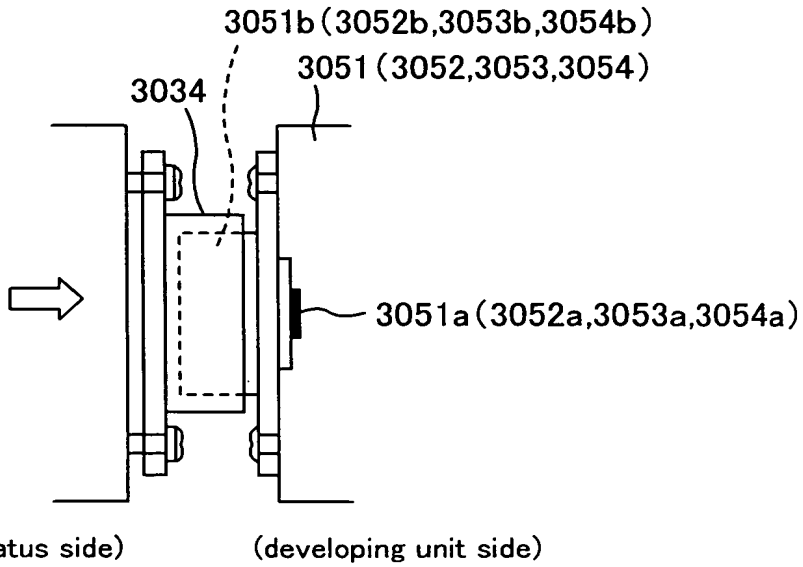


FIG. 22B



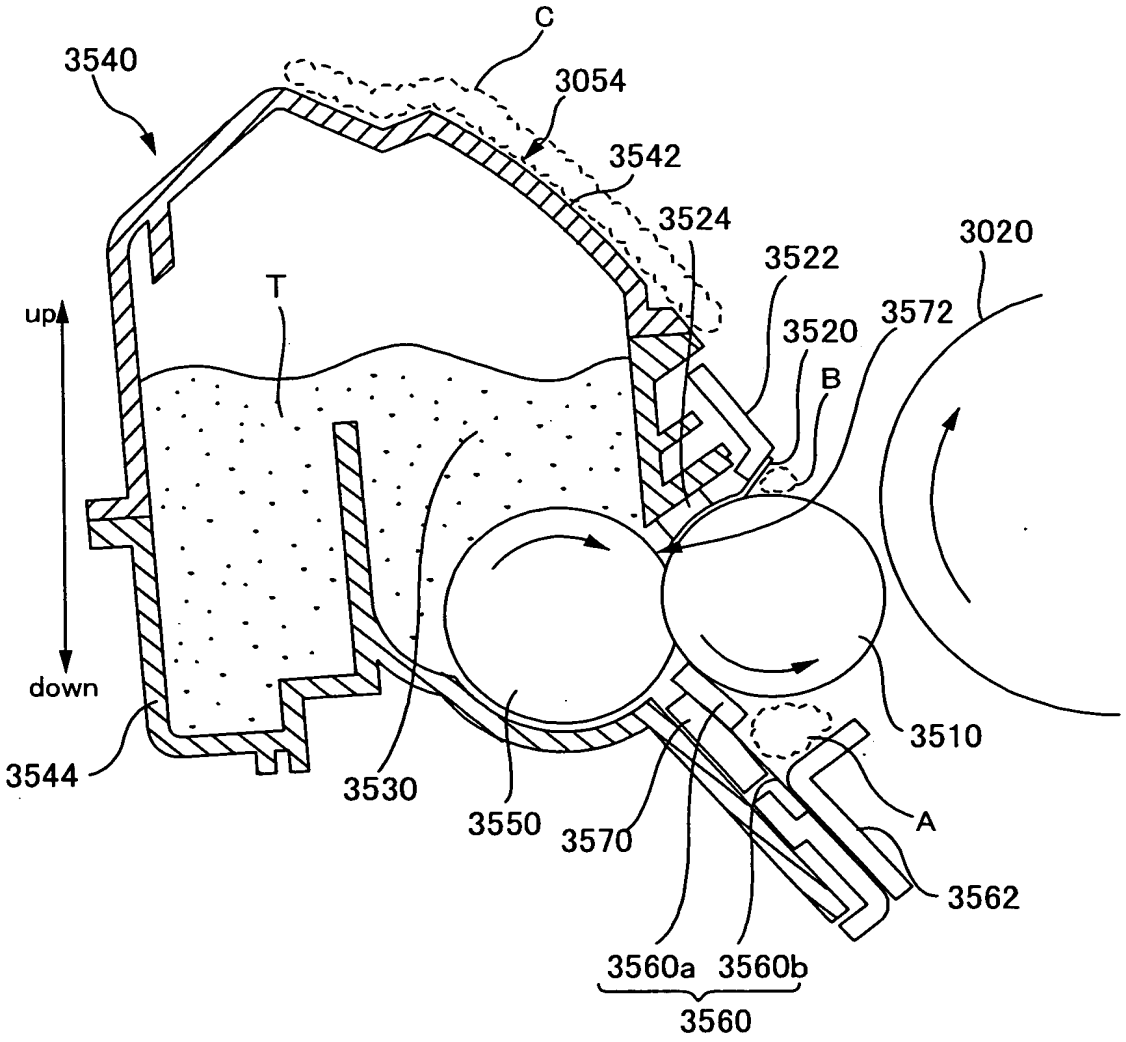

C
3540
3054
3542
3524
3522
3020
T
up
3520
3572
B
down
3544
3530
3550
3570
3510
A
3562
3560a
3560b
3560

FIG. 23

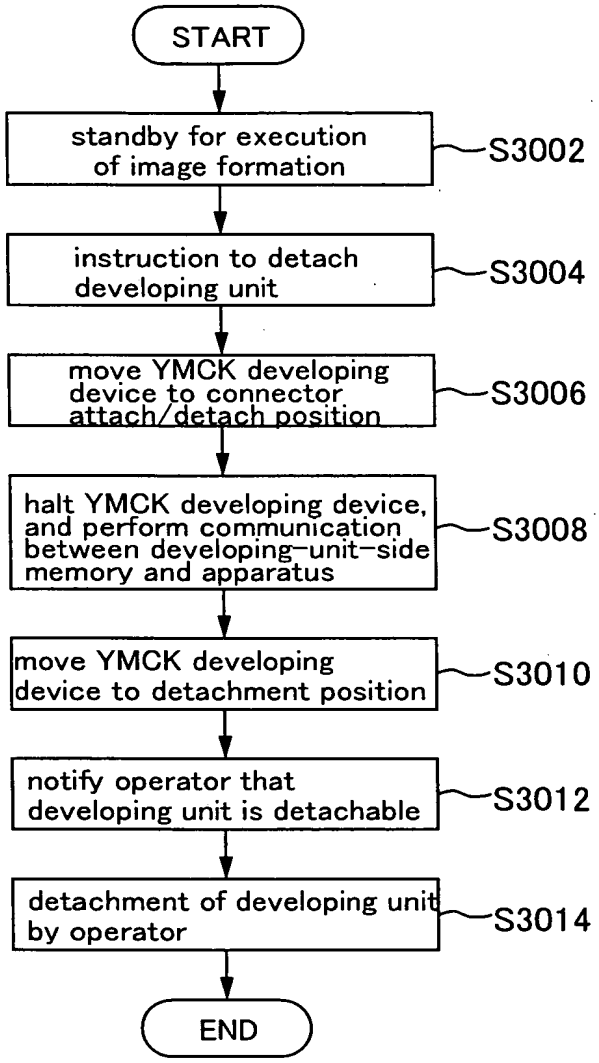

START
standby for execution of image formation
S3002
instruction to detach developing unit
S3004
move YMCK developing device to connector attach/detach position
S3006
halt YMCK developing device, and perform communication between developing-unit-side memory and apparatus
S3008
move YMCK developing device to detachment position
S3010
notify operator that developing unit is detachable
S3012
detachment of developing unit by operator
S3014
END

FIG. 24

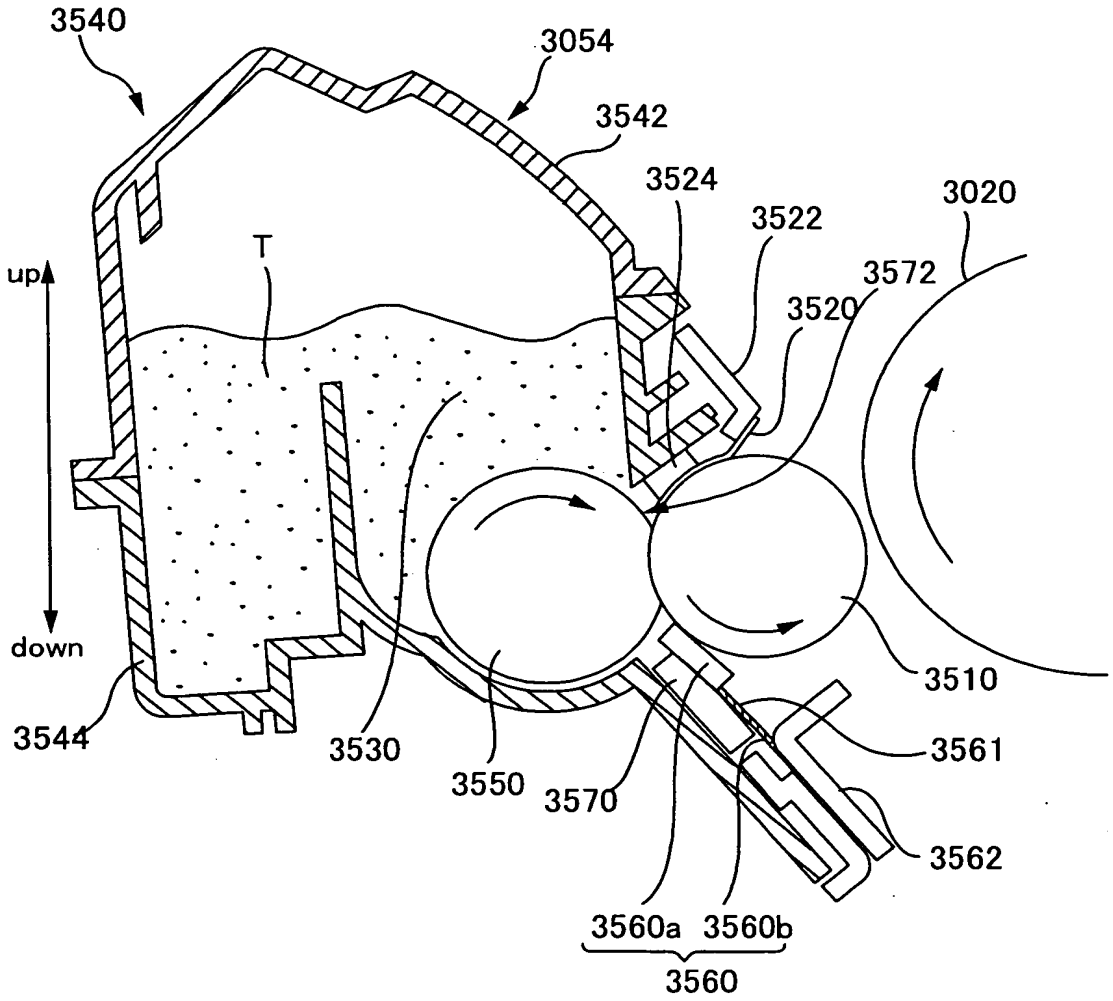

3540
3054
3542
3524
3522
3020
3572
3520
T
up
down
3544
3530
3550
3570
3510
3561
3562
3560a
3560b
3560

FIG. 25

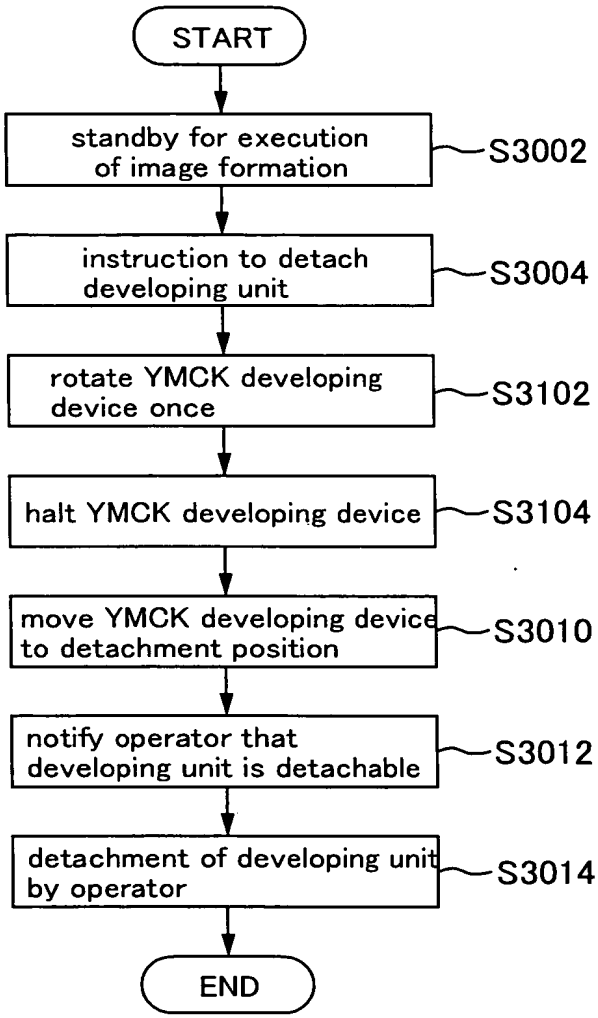

START
standby for execution of image formation
S3002
instruction to detach developing unit
S3004
rotate YMCK developing device once
S3102
halt YMCK developing device
S3104
move YMCK developing device to detachment position
S3010
notify operator that developing unit is detachable
S3012
detachment of developing unit by operator
S3014
END

FIG. 26

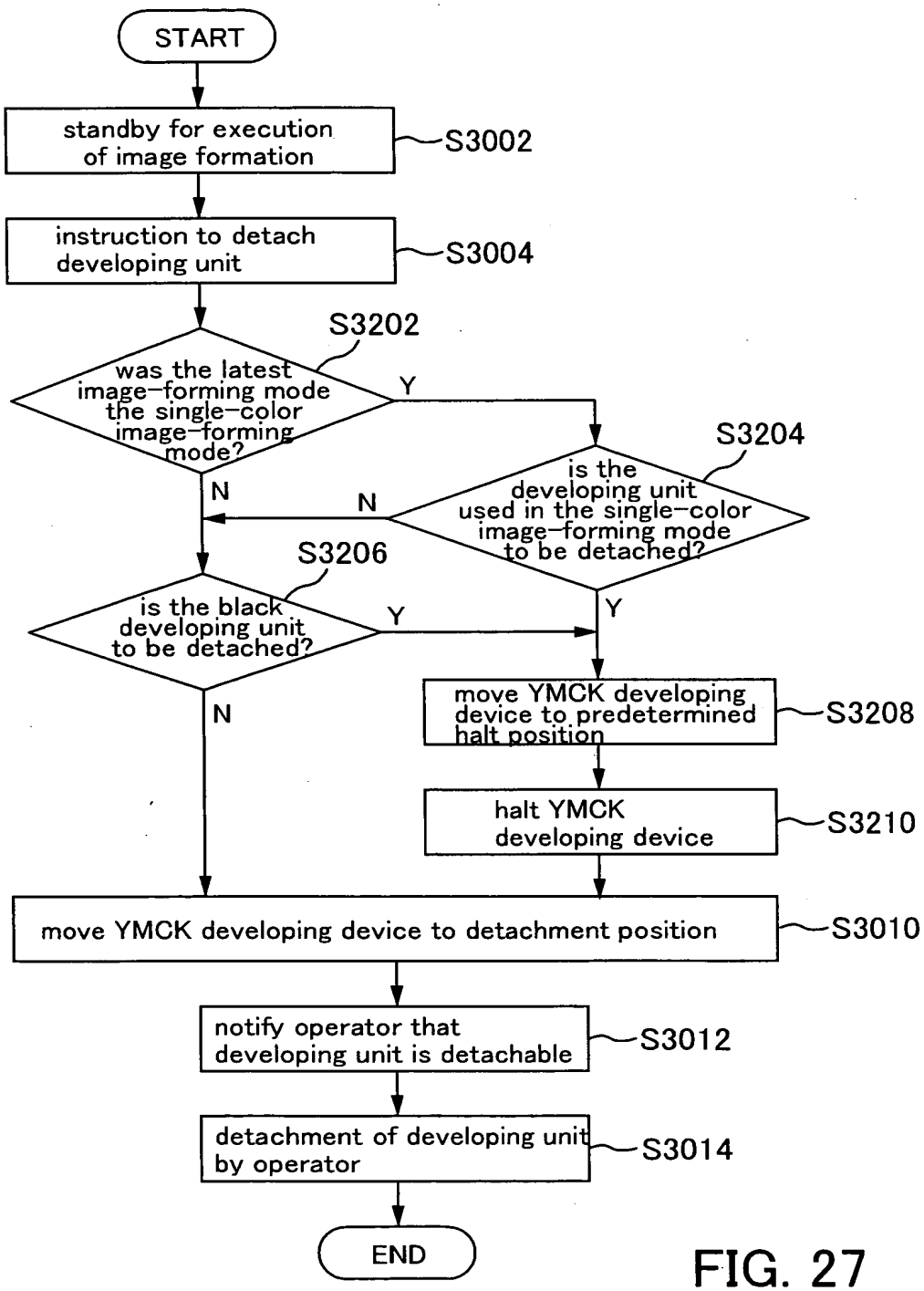

START
standby for execution of image formation
S3002
instruction to detach developing unit
S3004
S3202
was the latest image-forming mode the single-color image-forming mode?
Y
N
S3204
is the developing unit used in the single-color image-forming mode to be detached?
N
Y
S3206
is the black developing unit to be detached?
Y
N
move YMCK developing device to predetermined halt position
S3208
halt YMCK developing device
S3210
move YMCK developing device to detachment position
S3010
notify operator that developing unit is detachable
S3012
detachment of developing unit by operator
S3014
END

FIG. 27

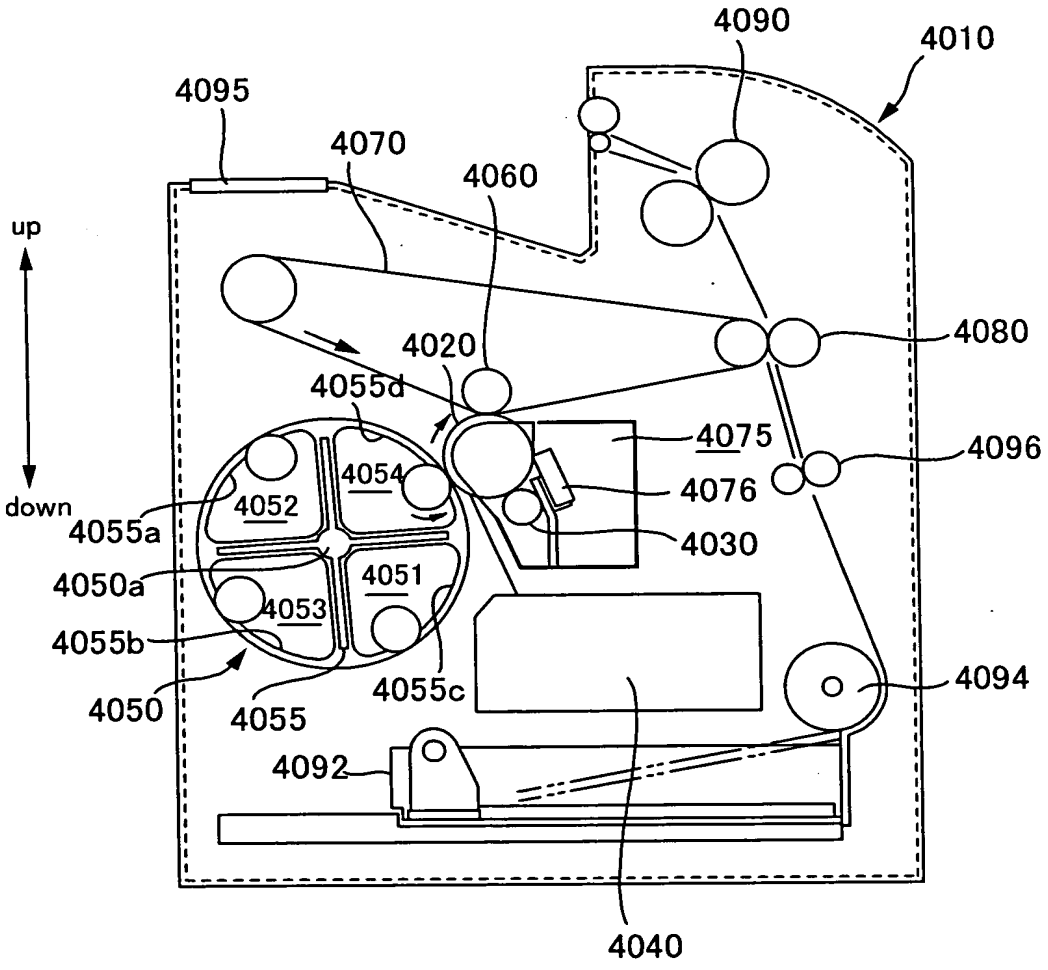

4090
4010
4095
4070
4060
up
4080
4020
4055d
4075
4096
4054
4076
down
4052
4055a
4030
4050a
4051
4053
4055b
4094
4050
4055
4055c
4092
4040

FIG. 28

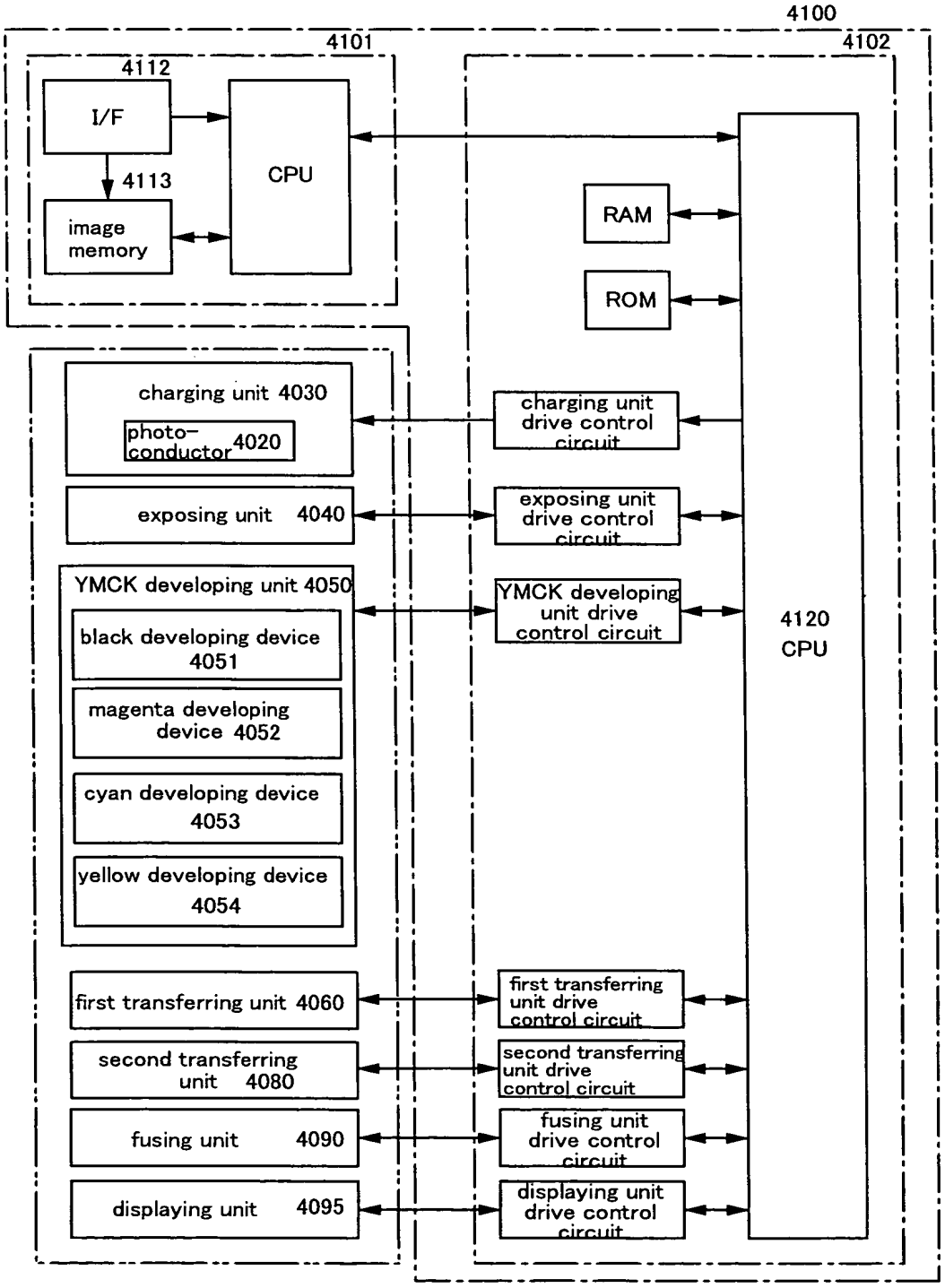

4100
4101
4102
4112
I/F
4113
image memory
CPU
RAM
ROM
charging unit 4030
photo-conductor 4020
charging unit drive control circuit
exposing unit 4040
exposing unit drive control circuit
YMCK developing unit 4050
black developing device 4051
magenta developing device 4052
cyan developing device 4053
yellow developing device 4054
YMCK developing unit drive control circuit
4120 CPU
first transferring unit 4060
first transferring unit drive control circuit
second transferring unit 4080
second transferring unit drive control circuit
fusing unit 4090
fusing unit drive control circuit
displaying unit 4095
displaying unit drive control circuit

FIG. 29

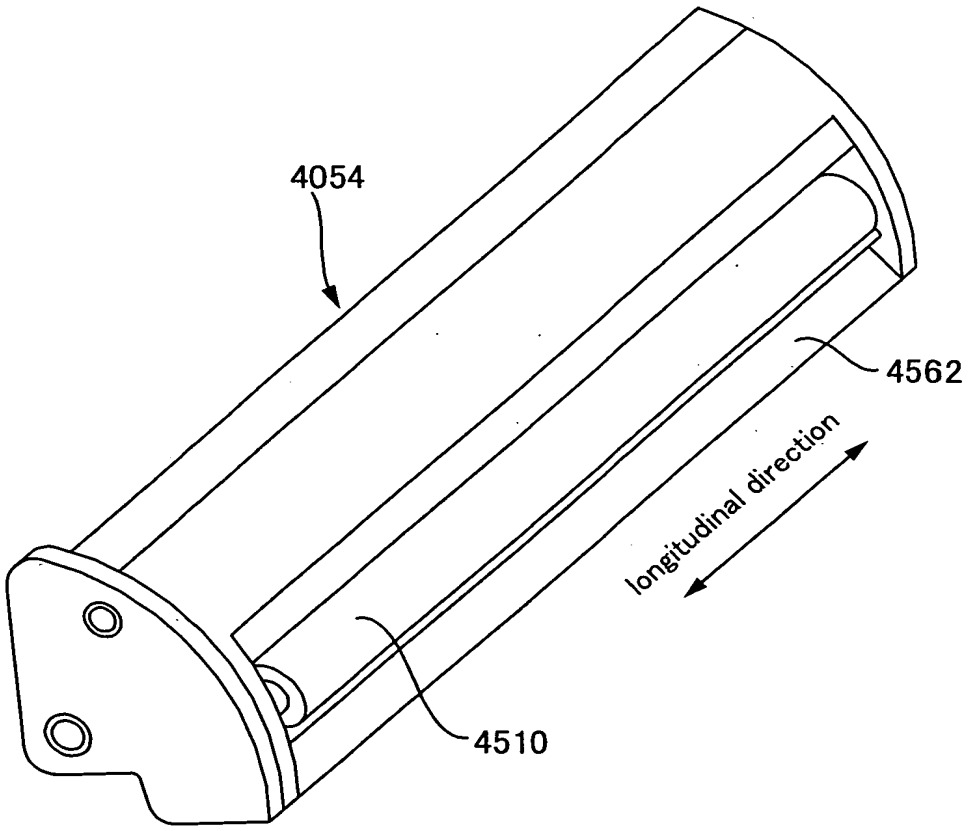


FIG. 30

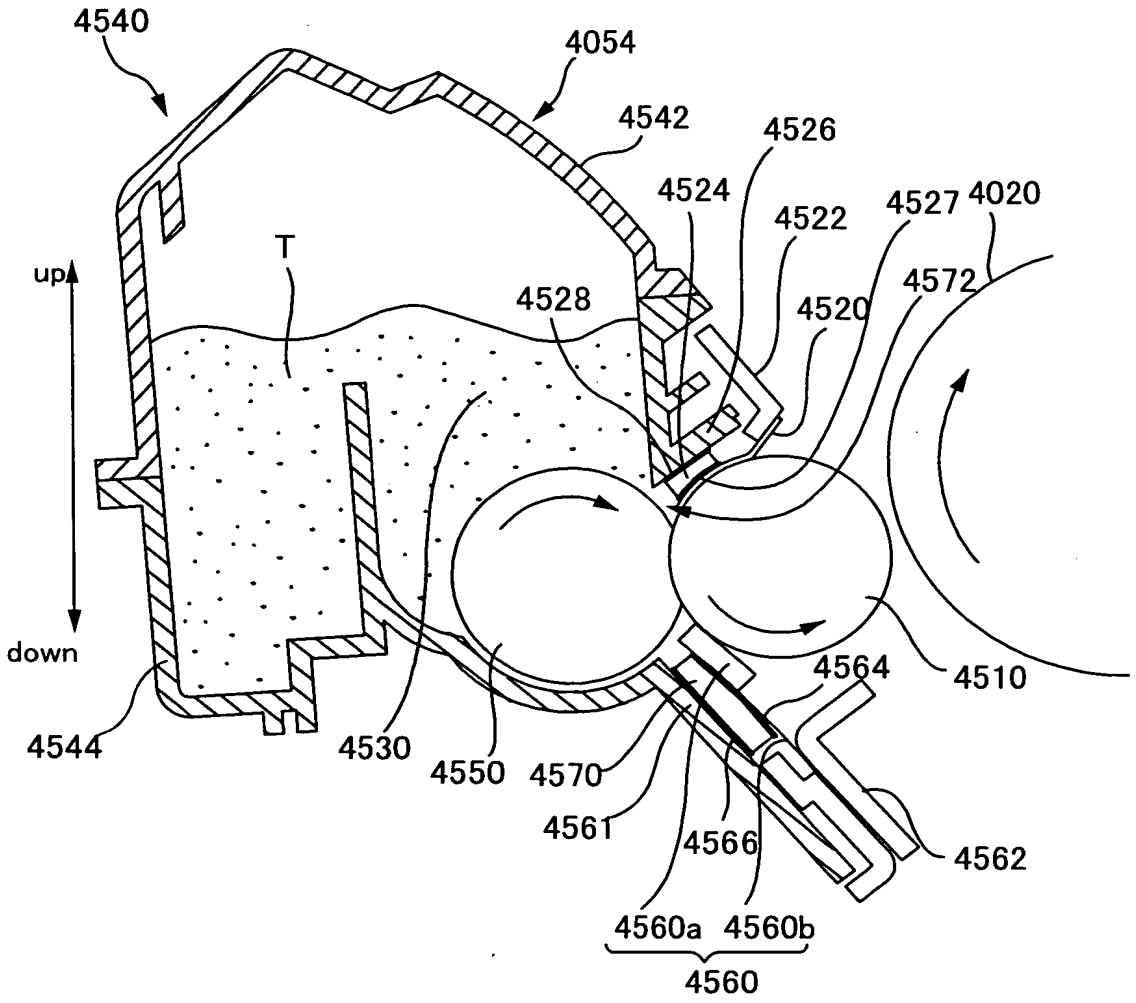

4540
4054
4542
4526
4524
4522
4527
4020
4572
4520
4528
T
up
down
4544
4530
4550
4570
4561
4566
4564
4510
4562
4560a
4560b
4560

FIG. 31

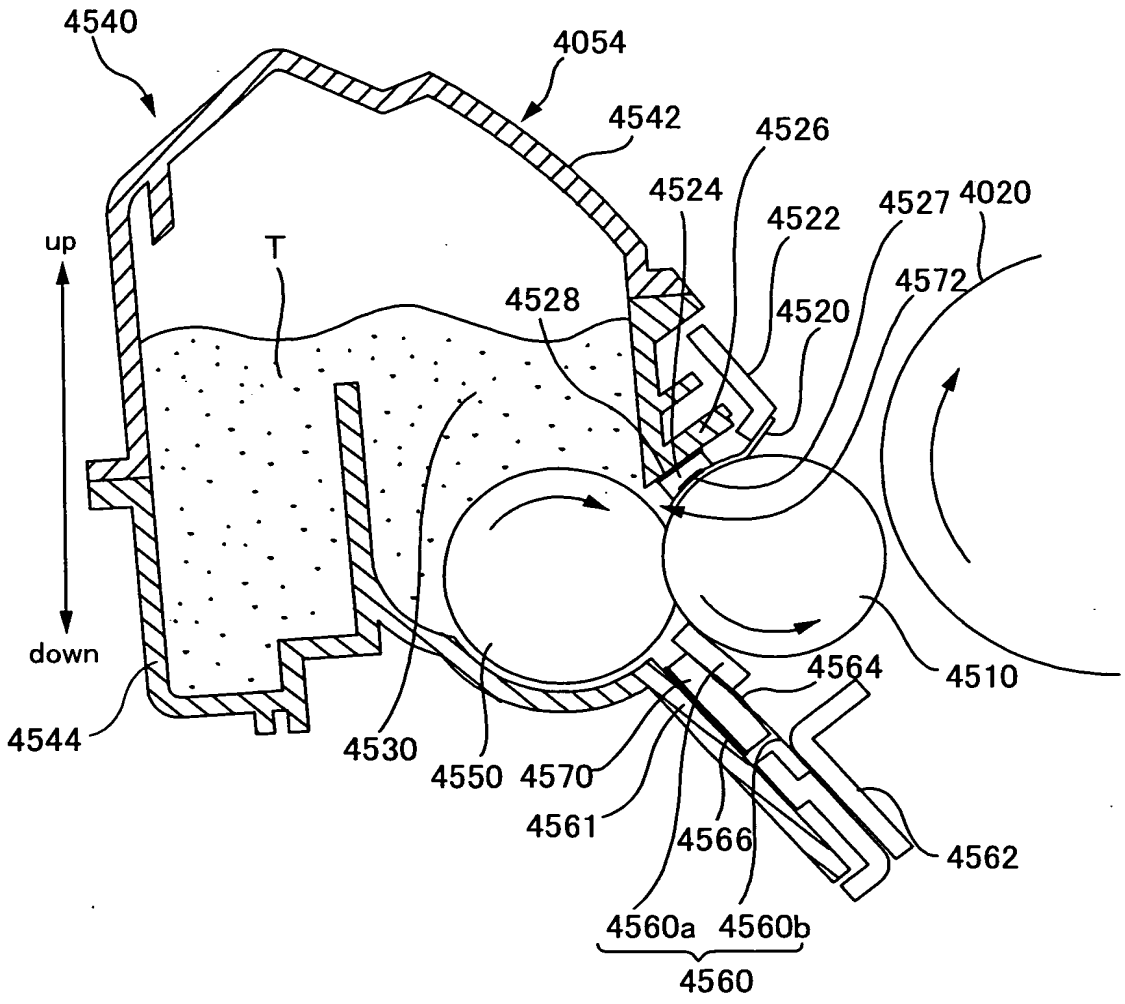

4540
4054
4542
4526
4524
4522
4527
4020
4572
4520
4528
T
up
down
4544
4530
4550
4570
4561
4566
4564
4510
4562
4560a
4560b
4560

FIG. 32

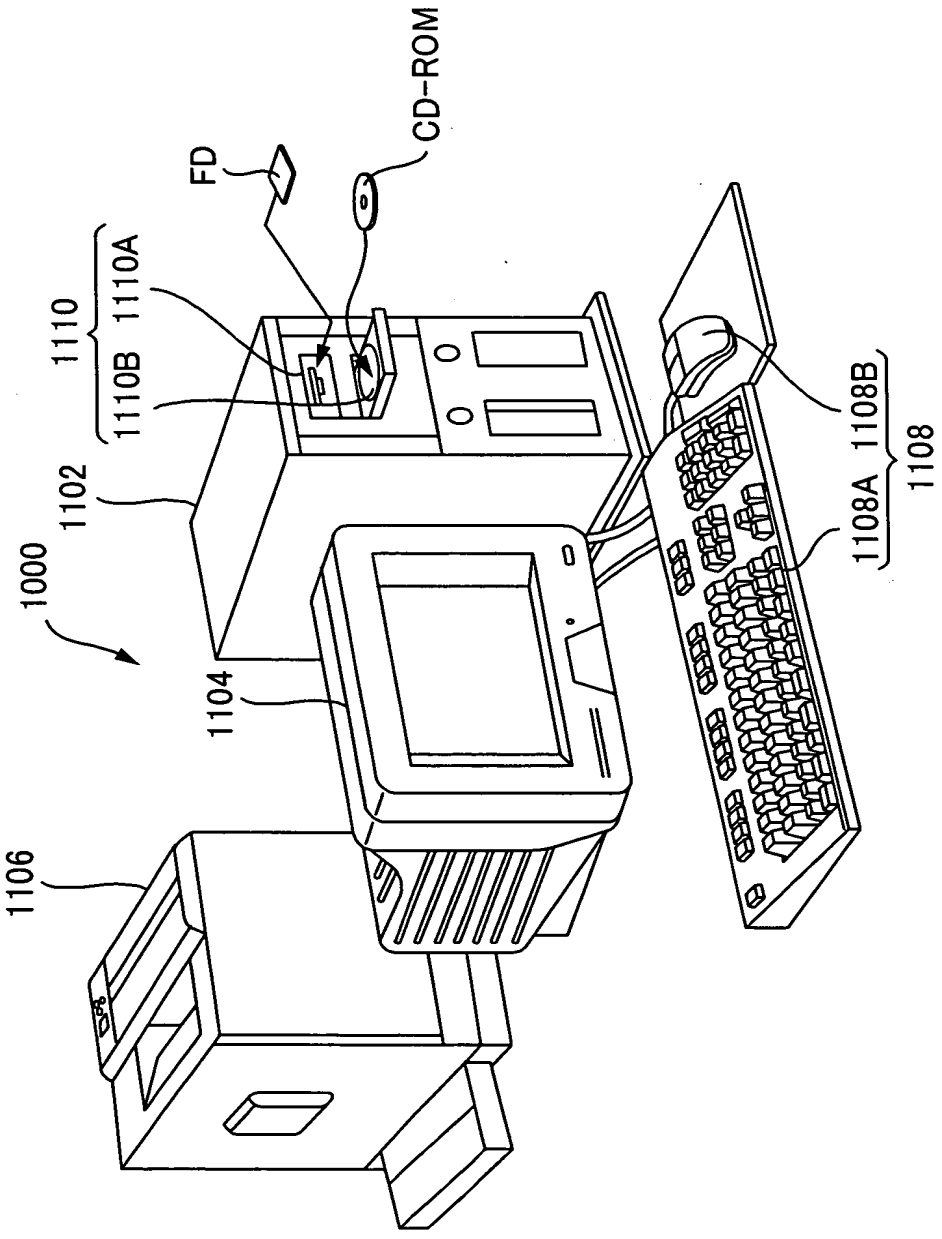

CD-ROM
FD
1110
1110A
1110B
1102
1000
1104
1106
1108B
1108A
1108

FIG. 33

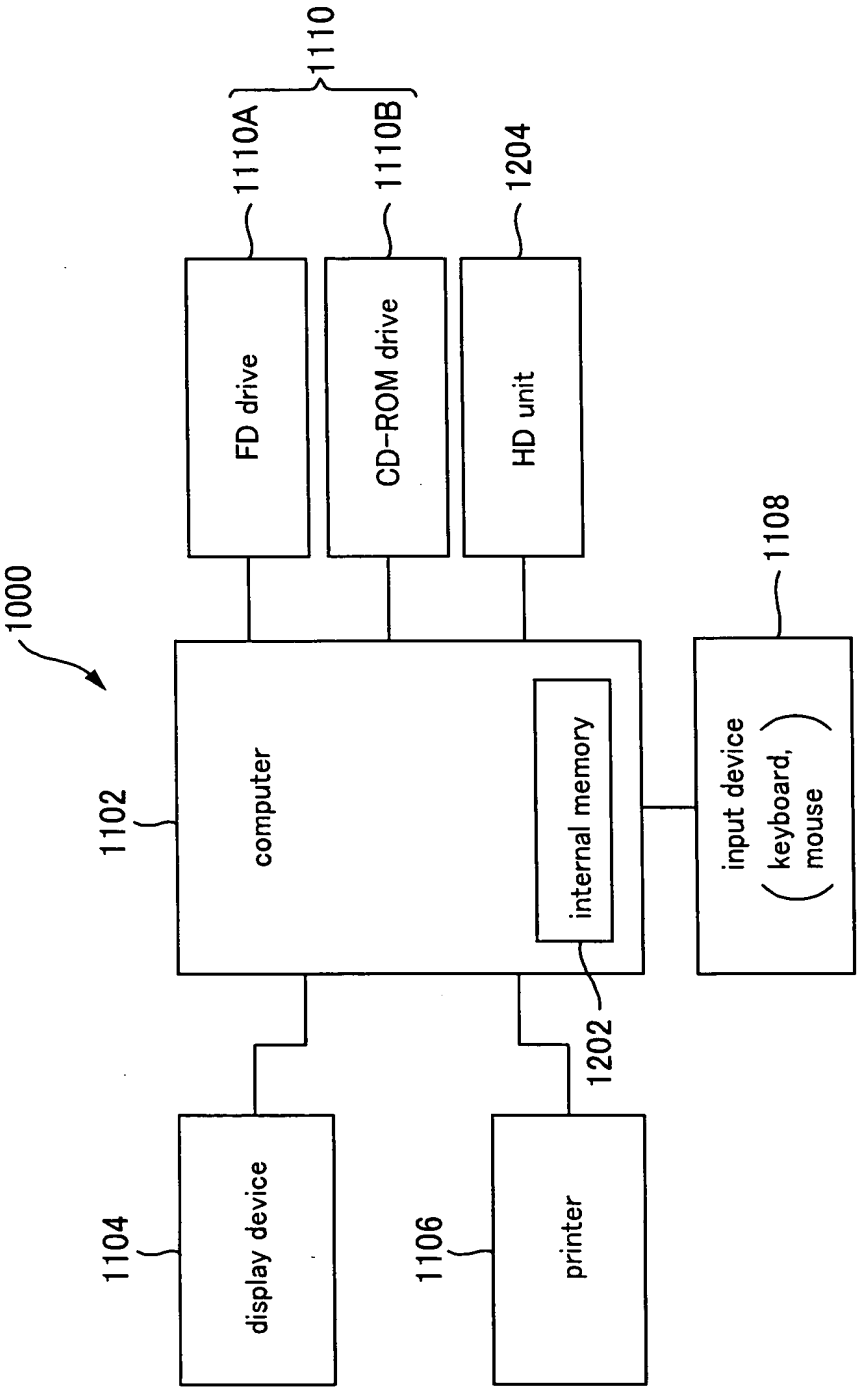

1000
1110
1110A
1110B
1204
FD drive
CD-ROM drive
HD unit
1108
computer
1102
internal memory
input device
(keyboard,
mouse)
1202
display device
1104
printer
1106

FIG. 34